VectraWave

PRODUCTS CATALOG

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CATALOG

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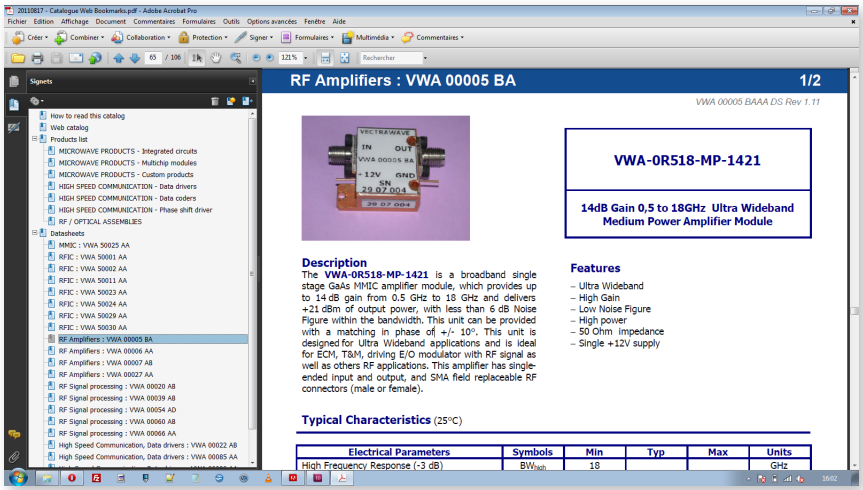

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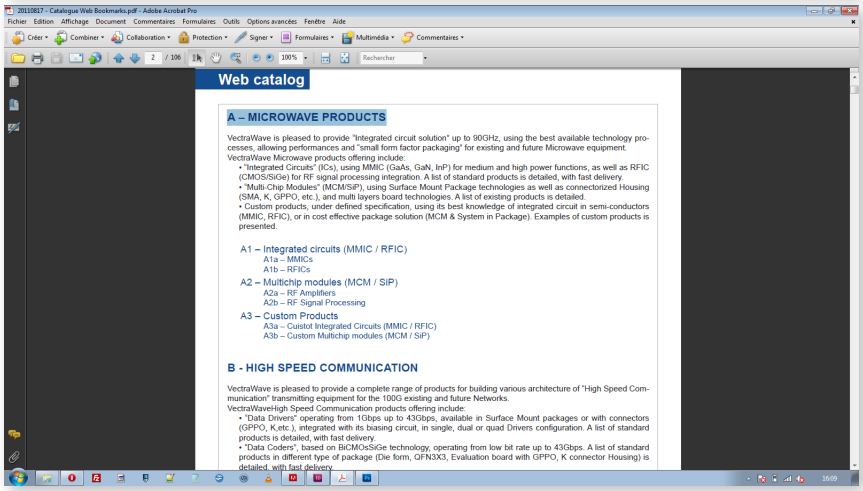

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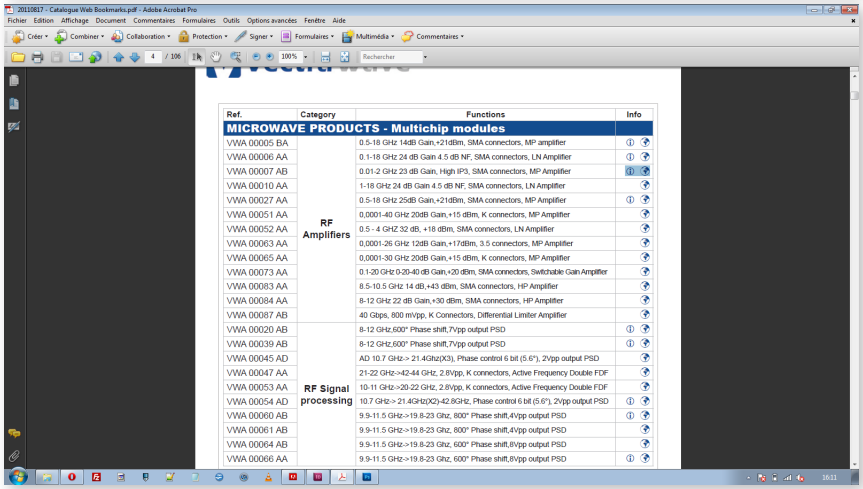


Web catalog

A – MICROWAVE PRODUCTS

VectraWave is pleased to provide “Integrated circuit solution” up to 90GHz, using the best available technology processes, allowing performances and “small form factor packaging” for existing and future Microwave equipment.
VectraWave Microwave products offering include:

- “Integrated Circuits” (ICs), using MMIC (GaAs, GaN, InP) for medium and high power functions, as well as RFIC (CMOS/SiGe) for RF signal processing integration. A list of standard products is detailed, with fast delivery.
- “Multi-Chip Modules” (MCM/SiP), using Surface Mount Package technologies as well as connectorized Housing (SMA, K, GPPO, etc.), and multi layers board technologies. A list of existing products is detailed.
- Custom products, under defined specification, using its best knowledge of integrated circuit in semi-conductors (MMIC, RFIC), or in cost effective package solution (MCM & System in Package). Examples of custom products is presented.

A1 – Integrated circuits (MMIC / RFIC)
A1a – MMICs
A1b – RFICs
A2 – Multichip modules (MCM / SiP)
A2a – RF Amplifiers
A2b – RF Signal Processing
A3 – Custom Products
A3a – Cuistot Integrated Circuits (MMIC / RFIC)
A3b – Custom Multichip modules (MCM / SiP)

B - HIGH SPEED COMMUNICATION

VectraWave is pleased to provide a complete range of products for building various architecture of “High Speed Communication” transmitting equipment for the 100G existing and future Networks.
VectraWaveHigh Speed Communication products offering include:

- “Data Drivers” operating from 1Gbps up to 43Gbps, available in Surface Mount packages or with connectors (GPPO, K,etc.), integrated with its biasing circuit, in single, dual or quad Drivers configuration. A list of standard products is detailed, with fast delivery.
- “Data Coders”, based on BiCMOsSiGe technology, operating from low bit rate up to 43Gbps. A list of standard products in different type of package (Die form, QFN3X3, Evaluation board with GPPO, K connector Housing) is detailed, with fast delivery.
- “Phase Shifter Drivers”, operating at 10.7G, 23G, 43G (others frequency can be discussed), ideal for the phase synchronization, delay and amplitude control of the clock signal of the equipment.A list of standard products is detailed, with fast delivery.

B1 – Data Drivers
B2 – Data Coders
B3 – Phase shift drivers

C - RF / OPTICAL ASSEMBLIES

Products list

Ref.	Category	Functions	Info
MICROWAVE PRODUCTS - Integrated circuits			
VWA 00081 AA	MMIC	8.5-10.5 GHz | 16 dB Gain | +40 dBm | HP Amplifier	
VWA 00082 AA		8-12 GHz | 22 dB Gain | +30 dBm | HP Amplifier	
VWA 50014 AA		DC-27 GHz | 17 dB Gain | + 21 dBm | MP Amplifier - 28Gb/s Driver 8Vpp	
VWA 50015 AA		DC-27 GHz | 17 dB Gain | + 21 dBm | MP Amplifier - 28Gb/s Driver 8Vpp	
VWA 50015 AB		DC-35 GHz | 10 dB Gain | +15 dBm | MP Amplifier - 40Gb/s Driver 3Vpp	
VWA 50015 AC		DC-35 GHz | 10 dB Gain | +15 dBm | MPA	
VWA 50025 AA		DC-45 GHz | 11 dB | +15 dBm Gain | LN Amplifier - 40Gb/s Driver 3 Vpp	
VWA 50028 AA		8.5-10.5 GHz | 16 dB Gain | +40 dBm | HP 2 stages Amplifier	
VWA 50035 AA		8-12.5 GHz | 22 dB Gain | +27 dBm | MPA 3 stages Amplifier	
VWA 50035 ACAA		8 to 12 GHz | 22 dB | 23 dBm | Single Bias Medium Power Amplifier MMIC	
VWA 50036 ACAA		8 to 12 GHz | 21 dB | 40 dBm | High Power Amplifier MMIC	
VWA 50042 AA		8 to 12 GHz | 25 dB | 12W | High Power Amplifier MMIC	
VWA 00055 AA	RFIC	30 Gbps | 800 mVpp | NRZ to RZ-DPSK coder	
VWA 00056 AA		30 Gbps | 800 mVpp | D - FF Gate	
VWA 00057 AA		0,1-30 GHz | Linear power controller | PC Amplifier	
VWA 00058 AA		30 Gbps | 800 mVpp | Duobinary Coder	
VWA 00059 AA		30 Gbps | 800 mVpp | NRZ to RZ Coder	
VWA 00074 AB		30 Gbps | 800 mVpp | Differential Coder	
VWA 00075 AB		30 Gbps | GPPO connectors | NRZ to RZ-DPSK Coder with Double Driver 7Vpp	
VWA 00077 AB		30 Gbps | 800 mVpp | GPPO connectors | NRZ to RZ-DPSK coder	
VWA 00078 AB		30 Gbps | 800 mVpp | GPPO Connectors | Differential Coder	
VWA 00088 AB		30 Gbps | 800 mVpp | GPPO Connectors | D - FF Gate	
VWA 00094 AA		30 Gbps | 800 mVpp | GPPO Connectors | Duobinary Coder	
VWA 00095 AA		30 Gbps | 800 mVpp | GPPO Connectors | NRZ to RZ Coder	
VWA 00096 AB		40 Gbps | 800 mVpp | Differential Limiter Amplifier	
VWA 50001 AA		40 Gbps | 800 mVpp | NRZ to RZ-DPSK coder	
VWA 50002 AA		40 Gbps | 800 mVpp | D - FF Gate	
VWA 50011 AA		0,1-30 GHz | Linear power controller | PC Amplifier	
VWA 50023 AA		40 Gbps | 800 mVpp | Differential Coder	
VWA 50024 AA		40 Gbps | 800 mVpp | NRZ to RZ Coder	
VWA 50029 AA		40 Gbps | 800 mVpp | Duobinary Coder	
VWA 50030 AA		40 Gbps | 800 mVpp | Differential Limiter Amplifier	
VWA 50057 AA		0,1-30 GHz | Linear power controller | PC Amplifier	

Ref.	Category	Functions	Info
MICROWAVE PRODUCTS - Multichip modules			
VWA 00005 BA	RF Amplifiers	0.5-18 GHz | 14dB Gain | +21dBm | SMA connectors | MP amplifier	
VWA 00006 AA		0.1-18 GHz | 24 dB Gain | 4.5 dB NF | SMA connectors | LN Amplifier	
VWA 00007 AB		0.01-2 GHz | 23 dB Gain | High IP3 | SMA connectors | MP Amplifier	
VWA 00010 AA		1-18 GHz | 24 dB Gain | 4.5 dB NF | SMA connectors | LN Amplifier	
VWA 00027 AA		0.5-18 GHz | 25dB Gain | +21dBm | SMA connectors | MP Amplifier	
VWA 00051 AA		0,0001-40 GHz | 20dB Gain | +15 dBm | K connectors | MP Amplifier	
VWA 00052 AA		0.5 - 4 GHZ | 32 dB | +18 dBm | SMA connectors | LN Amplifier	
VWA 00063 AA		0,0001-26 GHz | 12dB Gain | +17dBm | 3.5 connectors | MP Amplifier	
VWA 00065 AA		0,0001-30 GHz | 20dB Gain | +15 dBm | K connectors | MP Amplifier	
VWA 00073 AA		0.1-20 GHz | 0-20-40 dB Gain | +20 dBm | SMA connectors | Switchable Gain Amplifier	
VWA 00083 AA		8.5-10.5 GHz | 14 dB | +43 dBm | SMA connectors | HP Amplifier	
VWA 00084 AA		8-12 GHz | 22 dB Gain | +30 dBm | SMA connectors | HP Amplifier	
VWA 00087 AB		40 Gbps | 800 mVpp | K Connectors | Differential Limiter Amplifier	
VWA 000267 ABAA		8 5 to 11,5 GHz | 27 dB Gain | +39dBm | High Power Amplifier MMIC	
VWA 00020 AB	RF Signal processing	8-12 GHz | 600° Phase shift | 7Vpp output PSD	
VWA 00039 AB		8-12 GHz | 600° Phase shift | 7Vpp output PSD	
VWA 00045 AD		AD 10.7 GHz-> 21.4Ghz(X3) | Phase control 6 bit (5.6°) | 2Vpp output PSD	
VWA 00047 AA		21-22 GHz->42-44 GHz | 2.8Vpp | K connectors | Active Frequency Double FDF	
VWA 00053 AA		10-11 GHz->20-22 GHz | 2.8Vpp | K connectors | Active Frequency Double FDF	
VWA 00054 AD		10.7 GHz-> 21.4GHz(X2)-42.8GHz | Phase control 6 bit (5.6°) | 2Vpp output PSD	
VWA 00060 AB		9.9-11.5 GHz->19.8-23 Ghz | 800° Phase shift | 4Vpp output PSD	
VWA 00061 AB		9.9-11.5 GHz->19.8-23 Ghz | 800° Phase shift | 4Vpp output PSD	
VWA 00064 AB		9.9-11.5 GHz->19.8-23 Ghz | 600° Phase shift | 8Vpp output PSD	
VWA 00066 AA		9.9-11.5 GHz->19.8-23 Ghz | 600° Phase shift | 8Vpp output PSD	
VWA 0000104 AB		X to Ka band Filters Bank	

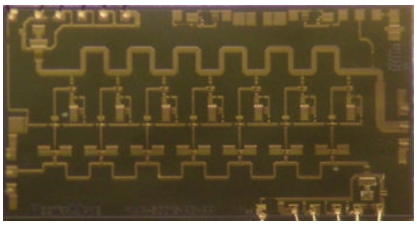
Ref.	Category	Info
MICROWAVE PRODUCTS - Custom products		
	Custom integrated circuits (MMIC / RFIC)	
	Custom integrated circuits (MCM / SiP)	

Ref.	Functions	Info
HIGH SPEED COMMUNICATION - Data drivers		
VWA 00022 AB	15 Gbps | 400 mVpp->8Vpp Output single Driver | SMA Housing	
VWA 00067 AA	28 Gbps | 400 mVpp->7/8 Vpp Output | GPPO connectors, Double Driver	
VWA 00085 AA	28 Gbps | 400 mVpp->7/8 Vpp Output | Single Driver	
VWA 00090 AA	28 Gbps | 400 mVpp->7/8 Vpp Output | Double Driver	
VWA 00091 AA	1-2 GHz | 20 dB Gain | 80 mA | Low Impedance | Laser Driver Amplifier LDA	
VWA 00091 AB	1-2 GHz | 20 dB Gain | 150 mA | Low Impedance | Laser Driver Amplifier LDA	
VWA 00099 AA	28 Gbps | 400 mVpp->7/8 Vpp Output | GPPO connectors | QUAD Driver	
VWA 00111 AA	32 Gbps | 400 mVpp->4/5 Vpp Output | Double Driver	
VWA 00112 AA	32 Gbps | 400 mVpp->4/5 Vpp Output | GPPO connectors | Double Driver	
VWA 00113 AA	32 Gbps | 400 mVpp->4/5 Vpp Output | GPPO connectors | QUAD Driver	

Ref.	Functions	Info
HIGH SPEED COMMUNICATION - Data coders		
VWA 00055 AA	30 Gbps | 800 mVpp | NRZ to RZ-DPSK coder	
VWA 00056 AA	30 Gbps | 800 mVpp | D - FF Gate	
VWA 00057 AA	40 Gbps | 800 mVpp | Differential Limiter Amplifier	
VWA 00058 AA	30 Gbps | 800 mVpp | Duobinary Coder	
VWA 00059 AA	30 Gbps | 800 mVpp | NRZ to RZ Coder	
VWA 00068 AB	40 Gbps | 800 mVpp | K connectors | NRZ to RZ-DPSK coder	
VWA 00069 AB	40 Gbps | 800 mVpp | K Connectors | D - FF Gate	
VWA 00070 AB	40 Gbps | 800 mVpp | K Connectors | Differential Coder	
VWA 00071 AB	40 Gbps | 800 mVpp | K Connectors | NRZ to RZ Coder	
VWA 00072 AB	40 Gbps | 800 mVpp | K Connectors | Duobinary Coder	
VWA 00074 AB	30 Gbps | 800 mVpp | Differential Coder	
VWA 00075 AB	30 Gbps | GPPO connectors | NRZ to RZ-DPSK Coder with Double Driver 7Vpp	
VWA 00077 AB	30 Gbps | 800 mVpp | GPPO connectors | NRZ to RZ-DPSK coder	
VWA 00078 AB	30 Gbps | 800 mVpp | GPPO Connectors, Differential Coder	
VWA 00087 AB	40 Gbps | 800 mVpp | K Connectors | Differential Limiter Amplifier	
VWA 00088 AB	30 Gbps | 800 mVpp | GPPO Connectors | D - FF Gate	
VWA 00094 AA	30 Gbps | 800 mVpp | GPPO Connectors | Duobinary Coder	
VWA 00095 AA	30 Gbps | 800 mVpp | GPPO Connectors | NRZ to RZ Coder	
VWA 50001 AA	40 Gbps | 800 mVpp | NRZ to RZ-DPSK coder	
VWA 50002 AA	40 Gbps | 800 mVpp | D - FF Gate	
VWA 50023 AA	40 Gbps | 800 mVpp | Differential Coder	
VWA 50024 AA	40 Gbps | 800 mVpp | NRZ to RZ Coder	
VWA 50029 AA	40 Gbps | 800 mVpp | Duobinary Coder	
VWA 50030 AA	40 Gbps | 800 mVpp | Differential Limiter Amplifier	

Ref.	Functions	Info
HIGH SPEED COMMUNICATION - Phase shift driver		
VWA 00020 AB	8-12 GHz | 600° Phase shift | 7Vpp output PSD	
VWA 00039 AB	8-12 GHz | 600° Phase shift | 7Vpp output PSD	
VWA 00045 AD	10.7 GHz-> 21.4Ghz(X3) | Phase control 6 bit (5.6°) | 2Vpp output PSD	
VWA 00047 AA	21-22 GHz->42-44 GHz | 2.8Vpp | K connectors | Active Frequency Double FDF	
VWA 00053 AA	10-11 GHz->20-22 GHz | 2.8Vpp | K connectors | Active Frequency Double FDF	
VWA 00054 AD	10.7 GHz-> 21.4GHz(X2)-42.8GHz | Phase control 6 bit (5.6°) | 2Vpp output PSD	
VWA 00060 AB	9.9-11.5 GHz->19.8-23 Ghz | 800° Phase shift | 4Vpp output PSD	
VWA 00061 AB	9.9-11.5 GHz->19.8-23 Ghz | 800° Phase shift | 4Vpp output PSD	
VWA 00064 AB	9.9-11.5 GHz->19.8-23 Ghz | 600° Phase shift | 8Vpp output PSD	
VWA 00066 AA	9.9-11.5 GHz->19.8-23 Ghz | 600° Phase shift | 8Vpp output PSD	

Ref.	Functions	Info
RF / OPTICAL ASSEMBLIES		
VLI 00005 AA	560 mA SOA | Driver for Optical Packet Switch OPS	
VLI 00005 AD	800 mA SOA | Driver for Optical Packet Switch OPS	



VWA-50025-AAAA

45 GHz – 11 dB – 16 dBm
Low Noise MMIC

Description

The **VWA-50025-AAAA** is an analog Low Noise/ medium power MMIC amplifier for ultra wide band applications up to 45GHz, with flat group delay.

The device is designed in 0.15µm low noise pHEMT process.

The devices is capable of more than +15 dBm output power at 1 dB compression point, and provide more than 11dB of gain from DC to 43 GHz with less than 1 dB of Gain variation with an excellent group delay up to 43GHz (less than +/- 3ps). The Design has been optimized to provide high efficiency, supply current is as low as 90mA with Vb=+8V.

The MMIC integrates an output power monitoring function: a 24 dB tap coupler delivers the image of the output level on a dedicated pad, and a peak detector is available on the die. Connecting the input of the peak detector to the tap coupler output will generate a DC signal, at the output of the detector, monitoring the output signal. A reference diode is also available for temperature stabilization of the detector function.

S2P file can be provided for system design simulation.

GDSII file is also available for mechanical design.

Features

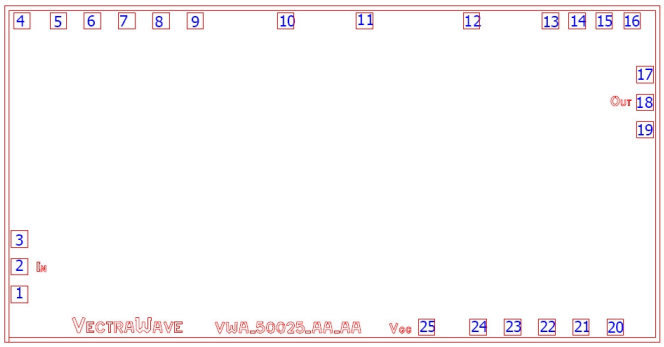
- LN pHEMT GaAs MMIC
- Wide band : DC – 43 GHz @ 1dB
- Flat group delay
- 50Ω RF Single ended input and output
- DC coupled
- Low power consumption <0,8W
- Positive voltage supply +8V
- Integrated output power tap coupler
- Integrated output level detection
- Reference diode output
- 2.97 x 1.52 x 0.10 mm

Applications

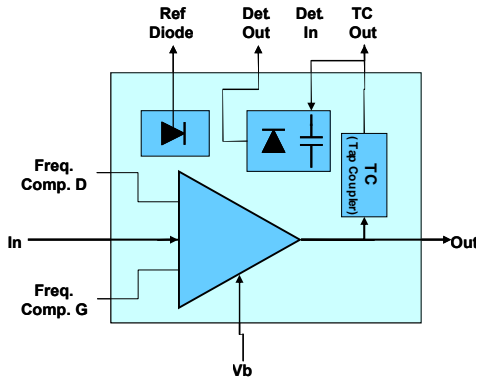
- Wide band Low Noise amplifier
- Radar / ECM / ECCM
- Test and measurement
- Fiber transmission: 10 to 50 Gbps
- Broadband communication

Ordering information

Product code
VWA 50025 AA



Pin out and dimensions
(2.97 X 1.52 X 0.10 mm)



Functional Block Diagram

Typical Characteristics: Tamb = 25°C, Vdd = +8V, Idd = 90mA.

Parameter	Symbol	Min	Typ	Max	Unit
Frequency range	F		45		GHz
Gain	G		11		dB
Gain flatness	ΔG		1		dB
Noise figure @ 10 GHz	NF		2		dB
Input adaptation	S11		12		dB
Output adaptation	S22		12		dB
Output power @ 1dB compression	P1dB		15		dBm
Saturated output power	PSat		16		dBm
Group delay variation	ΔΦ		+/- 3		ps
Output tap coupler ratio	TC		24		dB
Drain supply voltage	Vdd		8		V
Supply current	Idd		100		mA

Environment Parameters	Symbols	Min	Max	Units
Storage temperature	Tst	-65	+150	°C
Operating temperature	Top	-55	+85	°C

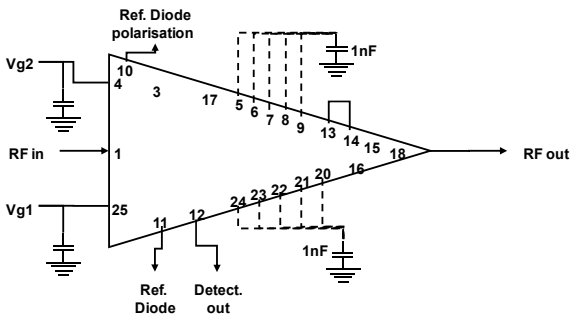
Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Positive External DC bias voltage	Vdd		9	V
RF input power (In)	Pin max		+20	dBm
Temperature process max 20 secondes	T process		325	°C
Continuous power dissipation (@ 85°C)	Pcw		0,8	W

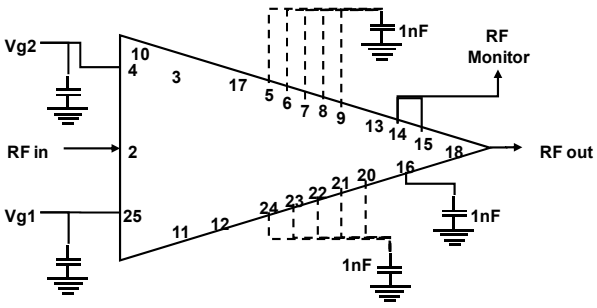
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Application circuit

with internal detector

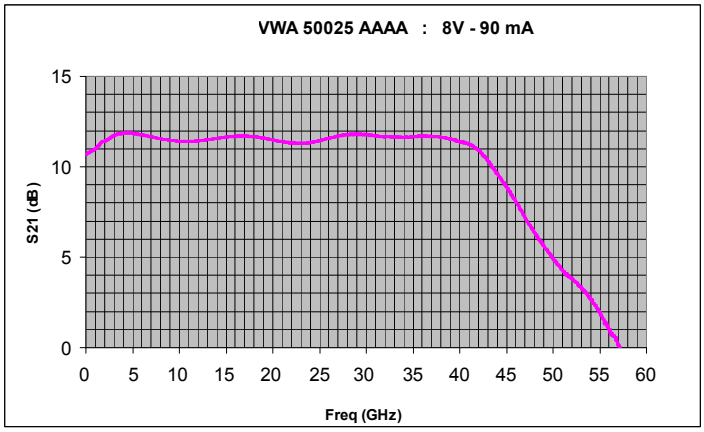


with external detector

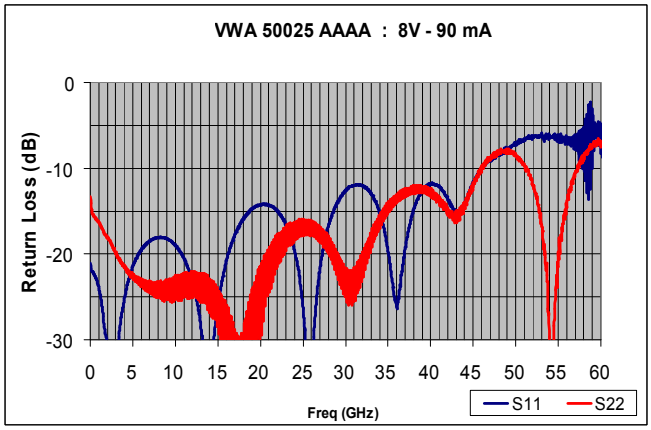


Probe measurement: Typical curves

Gain (dB) vs frequency (GHz)

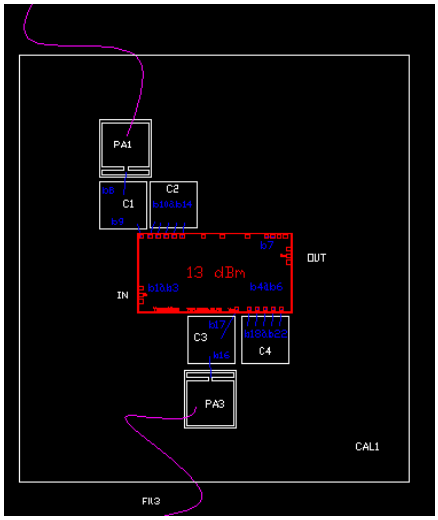


Return Loss (dB) vs frequency (GHz)

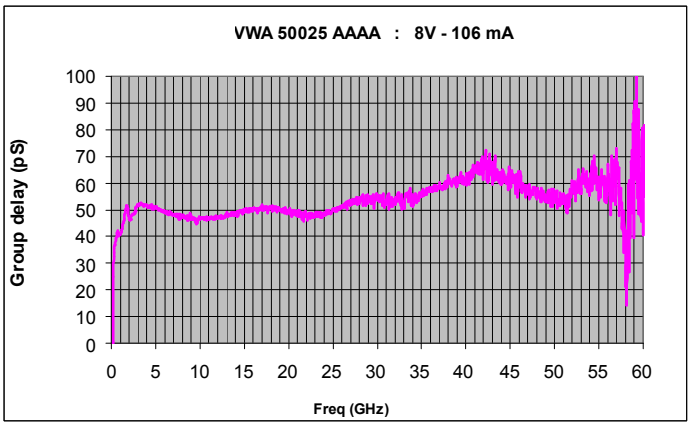


Probe Test configuration

C1, C2, C3, C4: 1000 pF capacitor

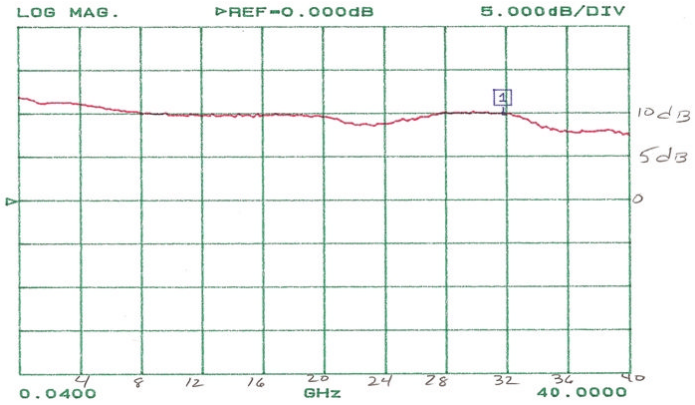


Group Delay (ps) vs frequency (GHz)

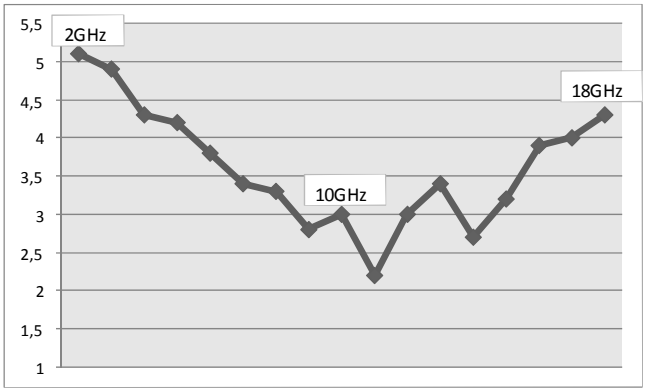


VWA 50025 AAAA Typical Performances in a "K Connector Evaluation Housing"

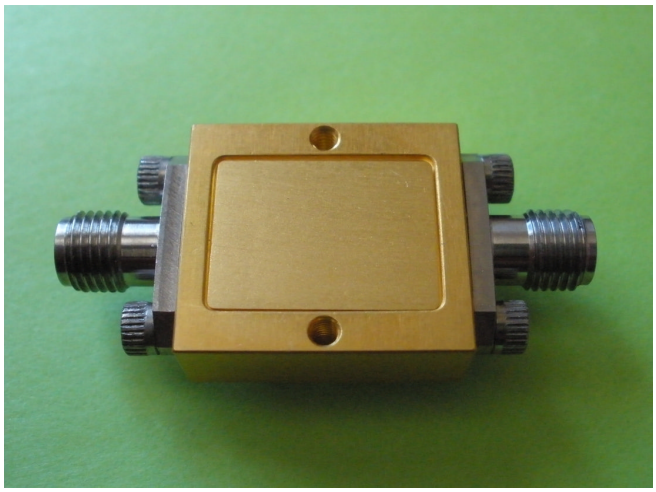
Gain (dB) vs frequency (GHz)



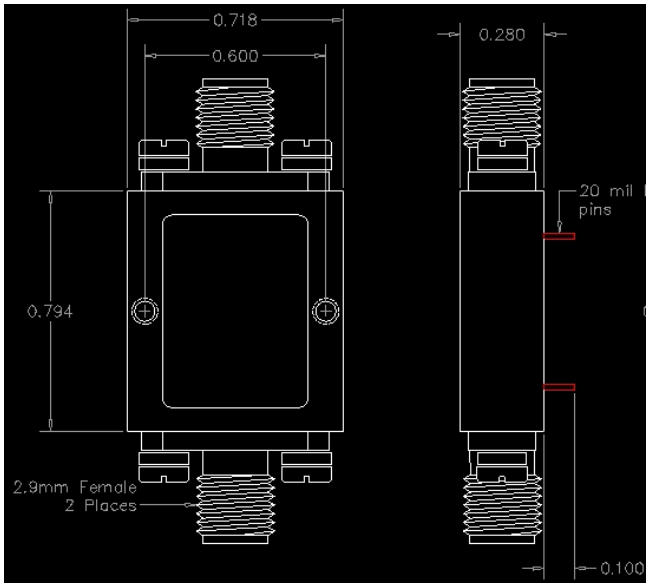
Noise Figure (dB) vs frequency (GHz)



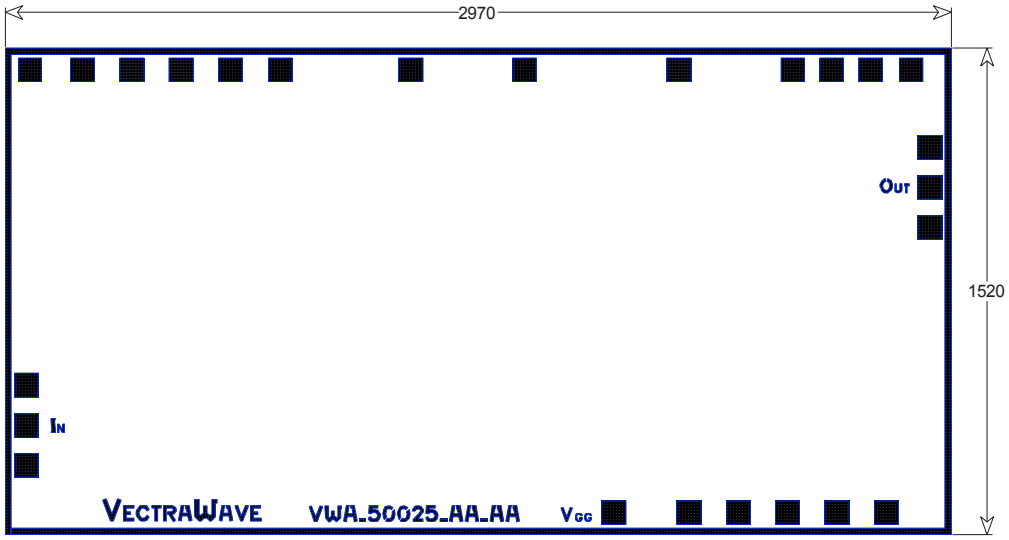
Top View



Dimensions



Pin out and pad description

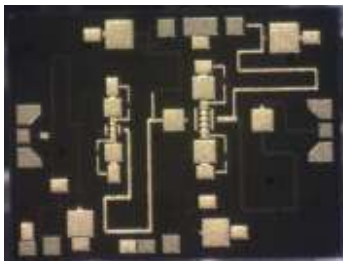


Pad #	Name	Description	Pad #	Name	Description
1	GND	Ground – for probe test	14	TC Out	Output power tap coupler
2	In	RF Input - DC coupled- 50Ohm matched	15	RFL	50 Ohm adaptation of TC out when used externally
3	GND	Ground – for probe test	16	C0	Connect to 1nF to ground when RFL is used
4	Vg2	Gate control 2 (positive volatge)	17	GND	Ground – for probe test
5	D0	Connect to 1nF to ground	18	Out	RF output - DC coupled- 50Ohm matched- Conect to Bias T
6	D1	Full band decoupling (same C as D0)	19	GND	Ground – for probe test
7	D2	Full band decoupling (same C as D0)	20	G0	Connect to 1nF to ground
8	D3	Full band decoupling (same C as D0)	21	G1	Full band decoupling (same C as G0)
9	D4	Full band decoupling (same C as D0)	22	G2	Full band decoupling (same C as G0)
10	VbDref	Polarization of reference diode –connect to	23	G3	Full band decoupling (same C as G0)
11	Dref	Reference diode …	24	G4	Full band decoupling (same C as G0)
12	Det Out	Output peak detector	25	Vg1	Gate control 1…(negtive voltage)
13	Det In	Input peak detector			

- All pads dimensions = 75 x 75 µm²; except pad 9 dimensions =100 x 100 µm²
- Die thickness = 100µm
- Die bottom must be connected to ground (RF and DC)

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50025-AA-AA** MMIC.



VWA-50035-ACAA

8 to 12 GHz – 22 dB – 23 dBm
Single Bias
Medium Power Amplifier MMIC

Description

The **VWA-50035-ACAAA** is an 2 Stages analog medium power MMIC amplifier operating in the frequency range 8 to 12 GHz.

The device is a cascaded 2 stages auto biased amplifier designed in 0.25µm pHEMT process.

The devices is capable of more than +24dBm output power at P sat, and provide more than 22dB of gain from 8 to 12 GHz with less than 1 dB of Gain variation. The Design has been optimized to provide high efficiency, supply current is as low as 120 mA with VD=+8V, when delivering +24dBm output power.

S2P file can be provided for system design simulation.

GDSII file is also available for mechanical design.

Features

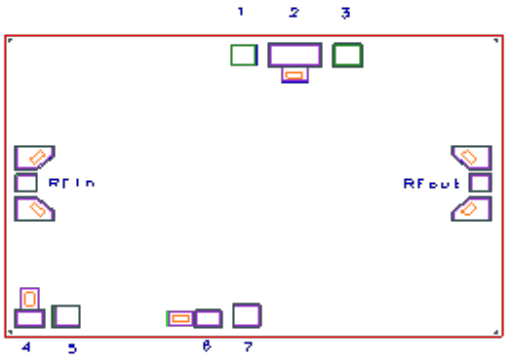
- 2 stages Medium Power pHEMT GaAs MMIC
- Single Bias, Low power consumption < 0,9W
- Wide band : 8 to 12 GHz
- High Output Psat : +24dBm
- High P1dB > + 22dBm
- High gain: 22dB min
- 50Ω, AC coupled RF input and output,
- Power supply: 120 mA @ +8 V
- Gain control capability in linear mode
- Small size: 1.97 x 1.47 x 0.10 mm

Applications

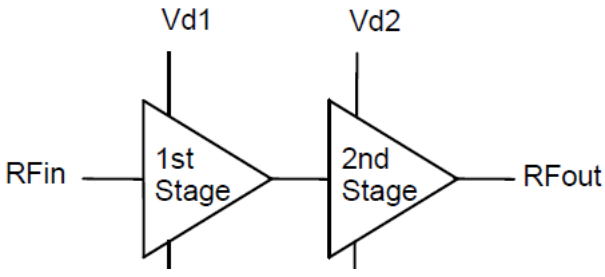
- X band Medium Power amplifier
- Radar / ECM / ECCM
- Test and measurement
- Broadband communication

Ordering information

Product code
VWA 50035 AC



Pin out and dimensions
(1.97 X 1.47 X 0.10 mm)



Functional Block Diagram

Typical Characteristics: Tamb = 25°C, Vdd = +8V, Idd = 120 mA.

Parameter	Symbol	Min	Typ	Max	Unit
Frequency range @3dB	F	7,5		13	GHz
Gain from 8 to 12 GHz	G	22	23		dB
Gain flatness from 8 to 12 GHz	ΔG		+/-0,5		dB
Noise figure @ 10 GHz	NF		7		dB
Input adaptation from 8 to 12 GHz	S11		10		dB
Output adaptation from 8 to 12 GHz	S22		10		dB
Output power @ 1dB compression	P1dB		22		dBm
Saturated output power	PSat		24		dBm
Drain supply voltage	Vdd		8		V
Supply current	Idd		120		mA

Environment Parameters	Symbols	Min	Max	Units
Storage temperature	Tst	-65	+150	°C
Operating temperature	Top	-55	+85	°C

Absolute maximum ratings

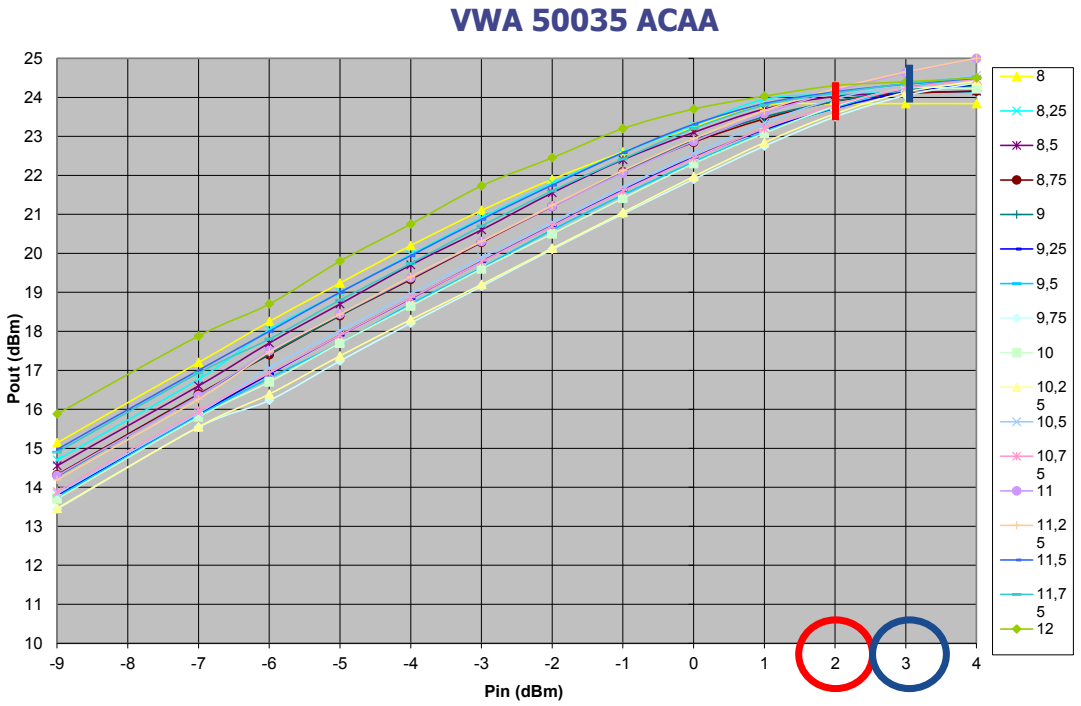
Maximum ratings	Symbols	Min	Max	Units
Positive External DC bias voltage	Vdd		8	V
RF input power (In)	Pin max		+20	dBm
Temperature process max 20 secondes	T process		325	°C
Continuous power dissipation (@ 85°C)	Pcw		1	W

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

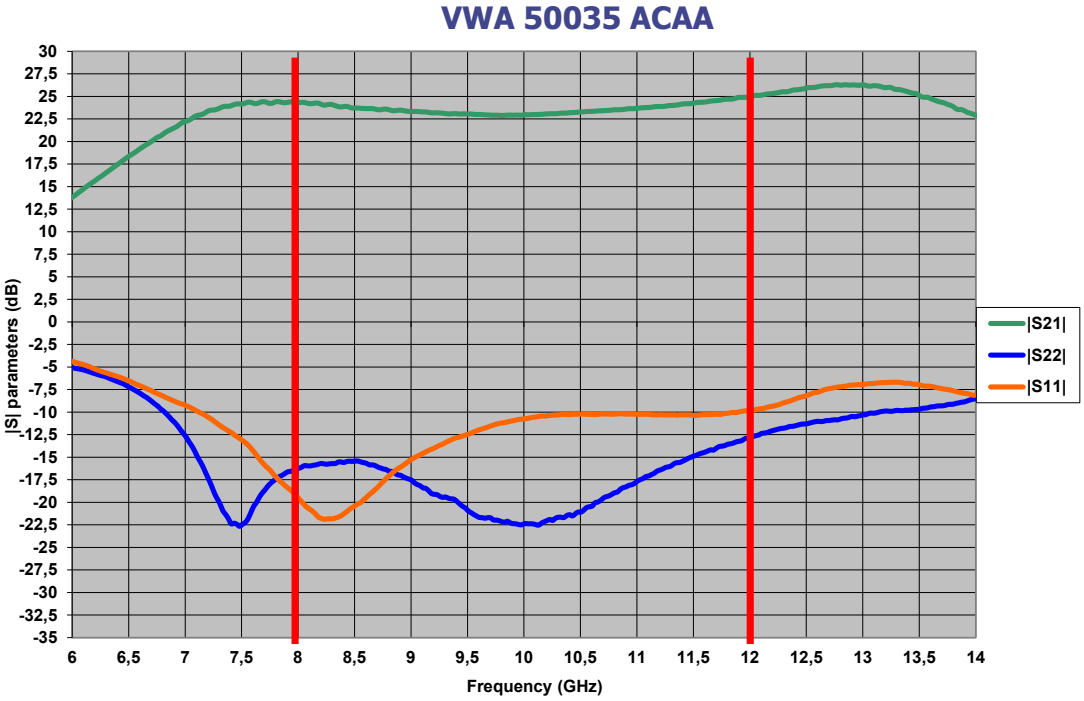
Application circuit: RF probe measurement

RF "Probe Measurement": Typical curves (VD=8v)

Pout function of frequency (GHz)

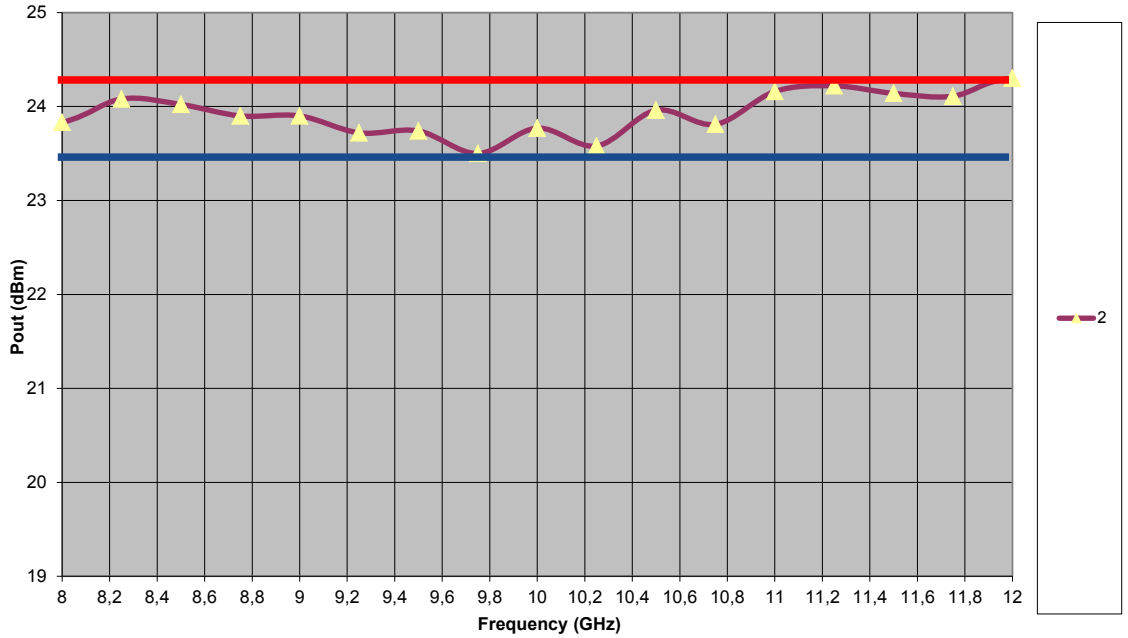


Small signal Gain and Input RL, Output RL function of frequency (GHz)

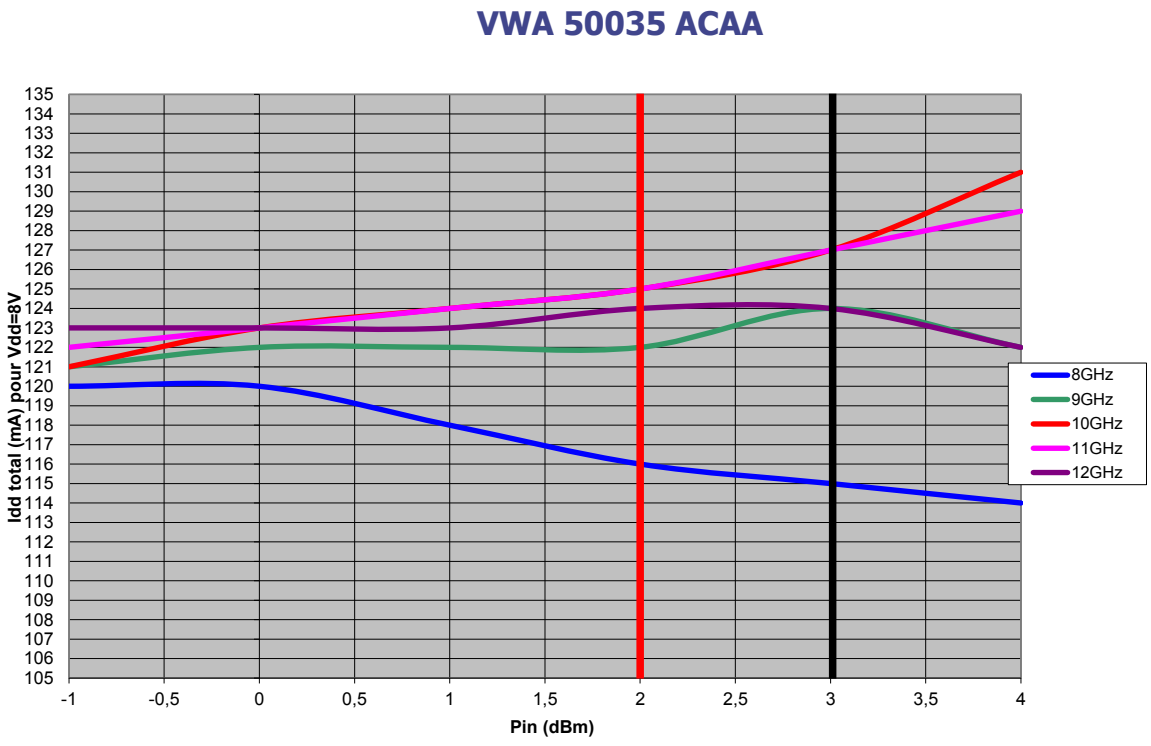


RF "Probe Measurement": Typical curves (VD=8v)

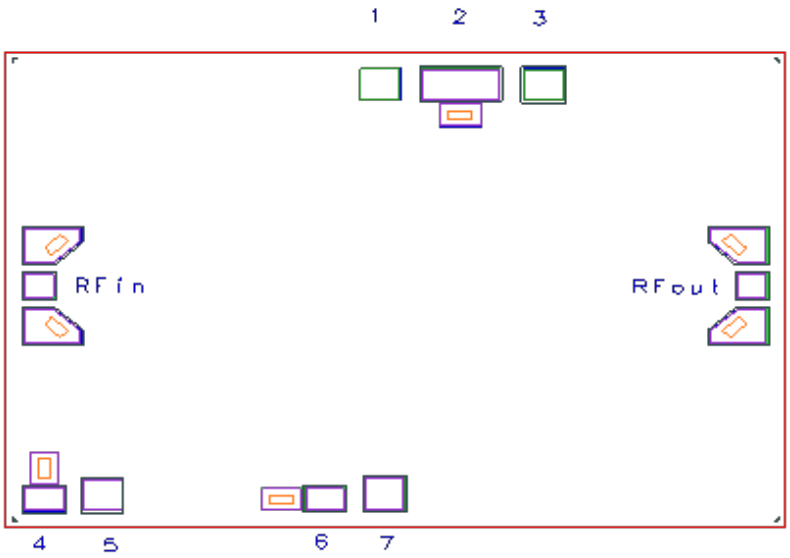
Pout function of Frequency for Pin =+2dBm



ID function of Pin and Frequency for VD=8V



Pin out and pad description



PAD	X (µm)	Y(µm)	Size(µm*µm)	Function
1	948	1370	100*100	Vd1
2	1149	1370	200*100	Gnd
3	1356	1370	100*100	Vd2
PAD RF IN	82	742	75*75	IN
PAD RF OUT	1880	742	75*75	OUT

- **Die size: 1.97 X 1.47 X 0.10 mm**
- All pads dimensions = 100 x 100 µm²; except pad 2 (200 X 100)
- RF in and RF out pad dimensions =75 x 75 µm²
- Die thickness = 100µm
- Die bottom must be connected to ground (RF and DC)

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50035-AC-AA** MMIC.

VWA-50036-ACAA

8 to 12 GHz – 21 dB – 40 dBm
High Power Amplifier MMIC

Description

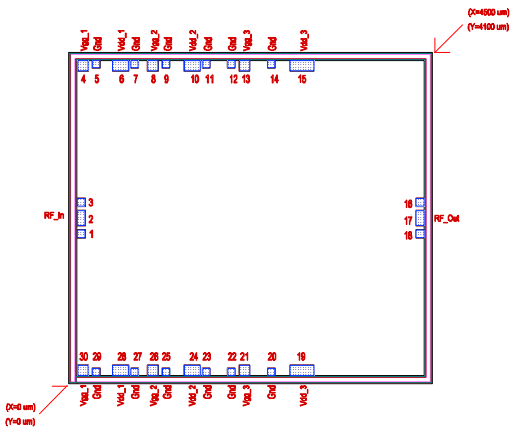
The **VWA-50036-ACAA** is a 3 Stages analog High power MMIC amplifier operating in the frequency range 8 to 13 GHz.

The device is a cascaded 3 stages amplifier designed in 0.25µm pHEMT process.

The devices is capable of more than +40,5 dBm output power at P sat, and provide more than 21dB of large signal gain from 8 to 12 GHz with less than 1 dB of Gain variation. The Design has been optimized to provide high efficiency, supply current is as low as 5 A with VD=+8V, when delivering +40,5dBm output power.

S2P file can be provided for system design simulation.

GDSII file is also available for mechanical design.



Pin out and dimensions
(4,5 X 4,1 X 0.10 mm)

Features

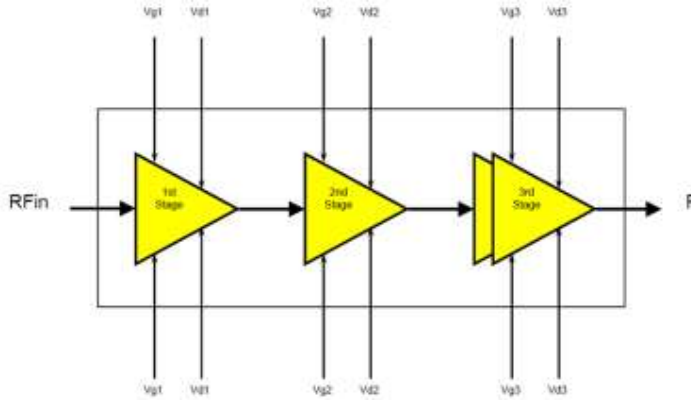
- 3 stages High Power pHEMT GaAs MMIC
- Wide band : 8 to 13 GHz
- High Output Psat > +40,5 dBm
- High P1dB > + 40dBm
- High large signal gain: 21dB min
- 50Ω, AC coupled RF input and output,
- Power supply: 5 A @ +8 V; Vg=-0,7 V
- 4,5 x 4,1 x 0.10 mm

Applications

- X band High Power amplifier
- Broadband communication
- Radar
- Test and measurement

Ordering information

Product code
VWA 50036 AC, Die
VWA 1000467ABAA, Die on carrier
VWA 1000054AHAA, carrier with power supply



Functional Block Diagram

Typical Characteristics: Tamb = 25°C, VD = +8V, ID = 5A (ID1N=ID1S=200 mA, ID2N=ID2S=600mA, ID3N=ID3S=1,8A), measured in pulsed mode for F= 10 KHz and duty cycle 10%.

Parameter measured in pulse mode	Symbol	Min	Typ	Max	Unit
Frequency range	F	8		13	GHz
Gain from 8 to 12 GHz	G	21	22		dB
Gain flatness from 8 to 12 GHz	ΔG		+/- 0,5		dB
Noise figure @ 10 GHz	NF		TBD		dB
Input adaptation from 8 to 12 GHz	S11		12		dB
Output adaptation from 8 to 12 GHz	S22		12		dB
Output power @ 1dB compression	P1dB	39,5		40,5	dBm
Saturated output power	PSat		40,5		dBm
Operating Drain supply voltage	VD	8		8,5	V
Supply current total	ID		5		A

Measurement reference planes are the INPUT and OUTPUT plans of the Die.

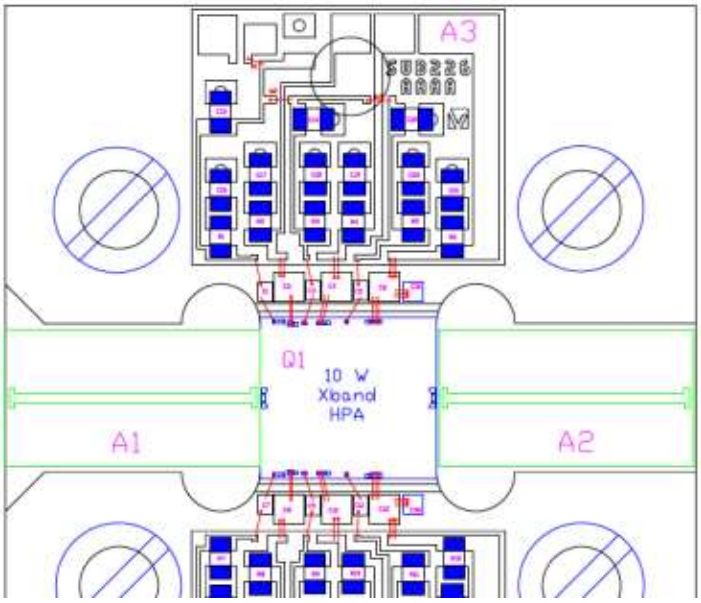
Environment Parameters	Symbols	Min	Max	Units
Storage temperature	Tst	-55	+85	°C
Operating temperature	Top	-40	+85	°C

Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Drain Voltage	VD		8,5	V
RF input power (In)	Pin max		+25	dBm
Temperature process max 20 secondes	T process		325	°C

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Application circuit:

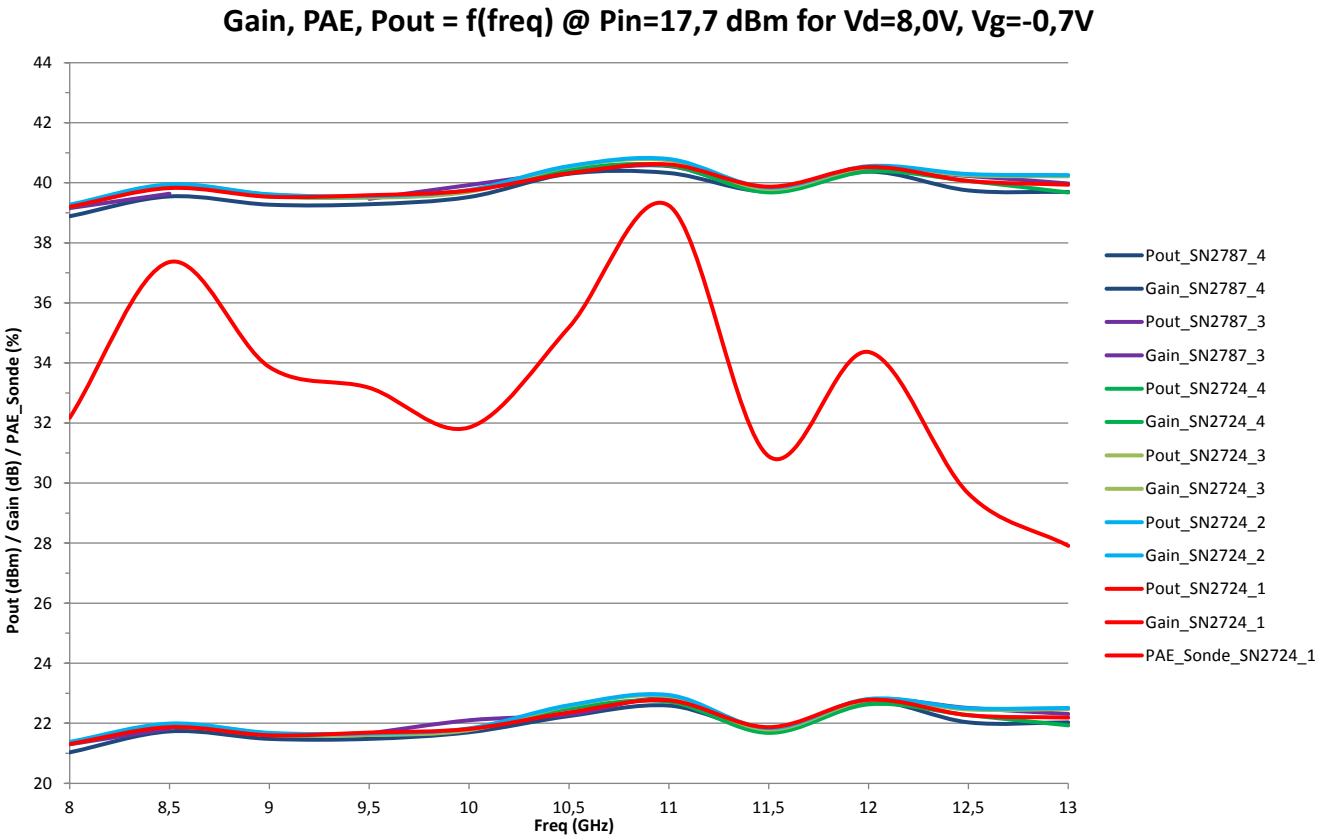


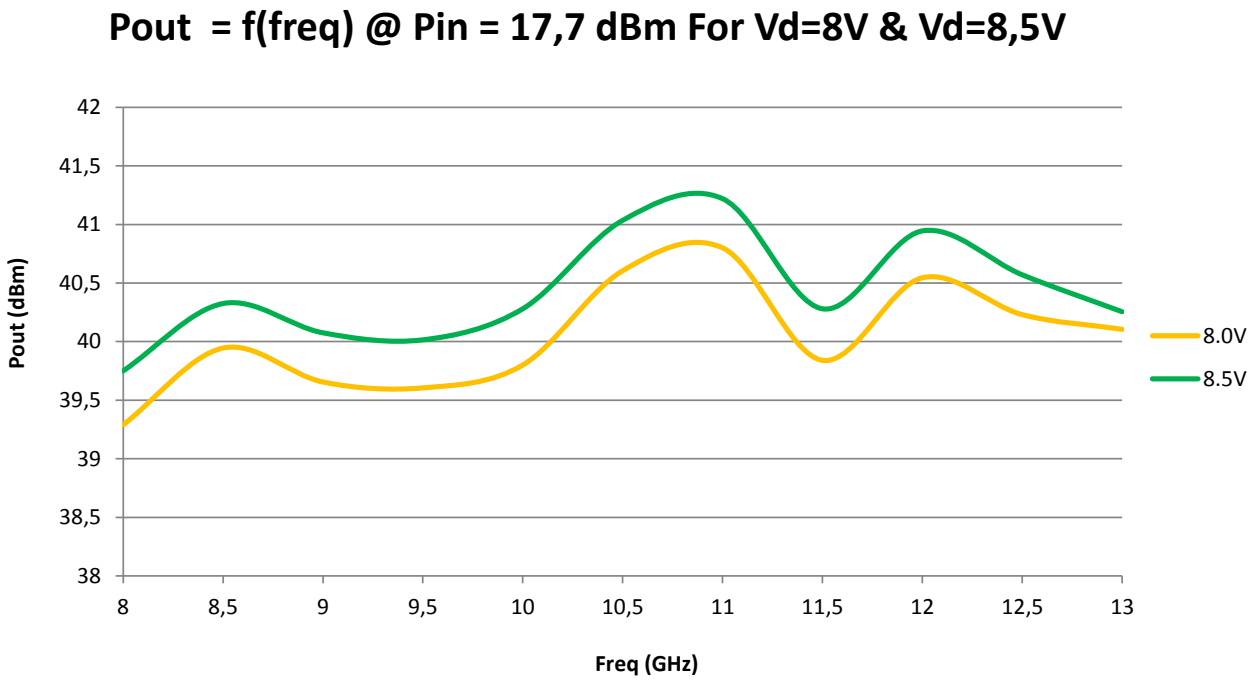
Die mounted on carrier

150pF	C1 C3 C5 C7 C9 C11
100pF	C2 C4 C6 C8 C10 C12
10nF	C16 C18 C20 C25 C27 C29
220nF	C17 C19 C21 C26 C28 C30
10nF	C31 C32
1µF	C13 C14 C15 C22 C23 C24
0Ω	R1 R3 R5 R7 R9 R11
11Ω	R2 R4 R6 R8 R10 R12

Table of Components mounted on the carrier

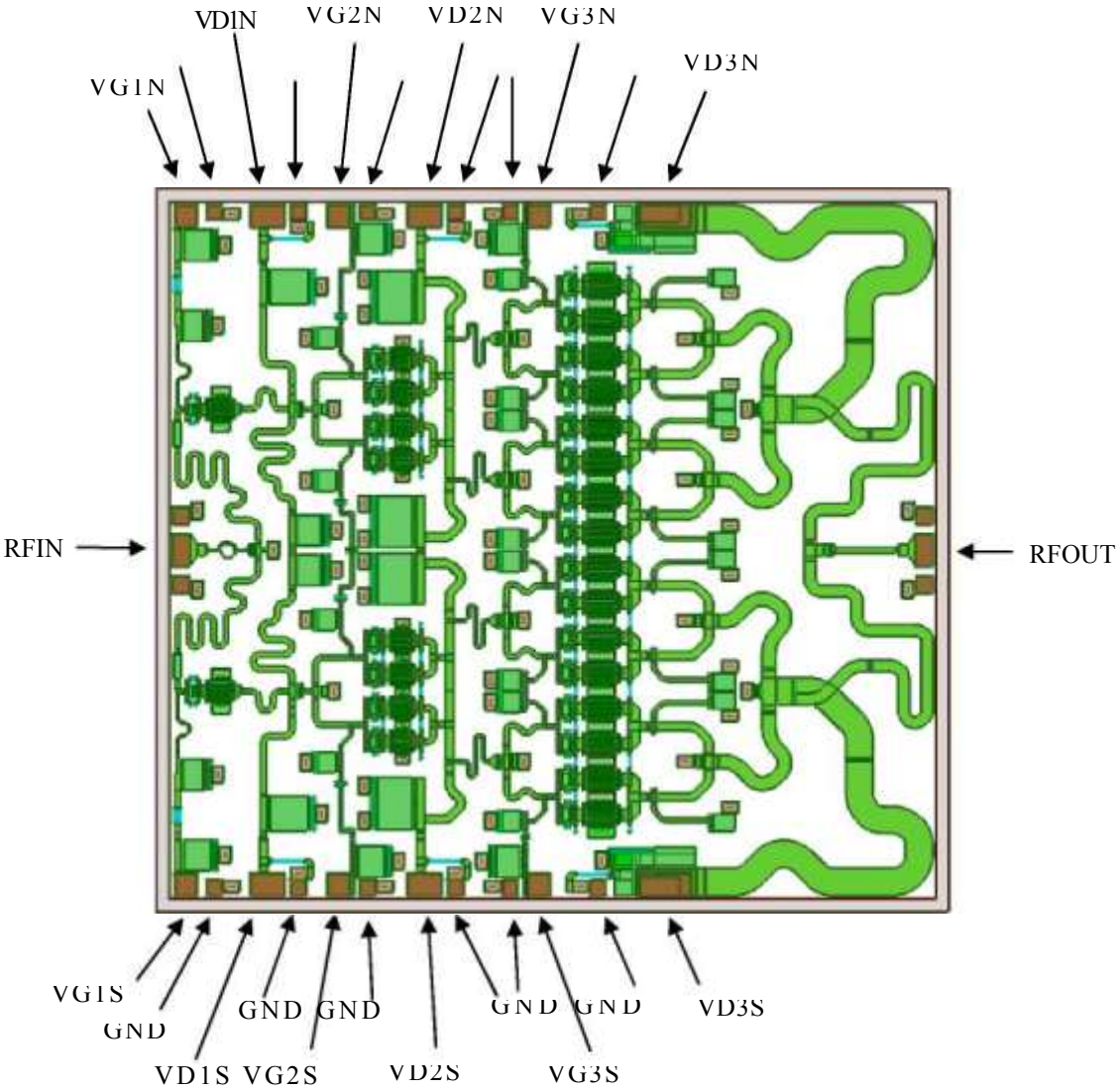
Typical test results in pulse mode





Die Lay out

The Die is symetrical on the RF axis. The die positionned top view with RF input on the left and RF output on the right show DC accesses on the top labelled north (N) and DC accesses on the bottom labelled south (S). VD1N, VD2N, VD3N, VG1N, VG2N, VG3N are DC signals applied on the north side, VD1S, VD2S, VD3S, VG1S, VG2S, VG3S are DC signals applied on the south side. Many ground accesses are complementing the pad layout. The backside is the ground reference plan.



Pin Out

The amplifier has a North face and a south face, north is top and south is bottom when RF input is on the left an RF output on the right.

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD1N	VD1N	First stage Drain (amplifier North)

VD2N	VD2N	Second stage Drain (amplifier North)
VD3N	VD3N	Third stage Drain (amplifier North)
VG1N	VG1N	First stage Gate (amplifier North)
VG2N	VG2N	Second stage Gate (amplifier North)
VG3N	VG3N	Third stage Gate (amplifier North)
VD1S	VD1S	First stage Drain (amplifier South)
VD2S	VD2S	Second stage Drain (amplifier South)
VD3S	VD3S	Third stage Drain (amplifier South)
VG1S	VG1S	First stage Gate (amplifier South)
VG2S	VG2S	Second stage Gate (amplifier South)
VG3S	VG3S	Third stage Gate (amplifier South)
GND	BACKSIDE	Ground

Bonding Pad Coordinates

Symbol	X coordinate (µm)	Y coordinate (µm)	Pad size (µm x µm)
GND	90	1850	Ground pad associated with RF input
RFIN	90	2050	100 x 190
GND	90	2250	Ground pad associated with RF input
VG1N	115	3995	130 x 130
GND	280	4015	90 x 90
VD1N	595	3995	200 x 130
GND	771	4015	90 x 90
VG2N	1005	3995	130 x 130
GND	1170	4015	90 x 90
VD2N	1506	3995	200 x 130
GND	1684	4015	90 x 90
GND	2005	4015	90 x 90
VG3N	2170	3995	130 x 130
GND	2522	4015	90 x 90
VD3N	2914	3995	300 x 100
GND	4410	1850	Ground pad associated with RF output
RFOUT	4410	2050	100 x 190
GND	4410	2250	Ground pad associated with RF output
GND	BACKSIDE		Ground

Bonding Pad Drawing

MMIC Steps on the wafer are 4.5 and 4.1 mm along X and Y coordinated respectively, dicing typically reduce the die by 30um.

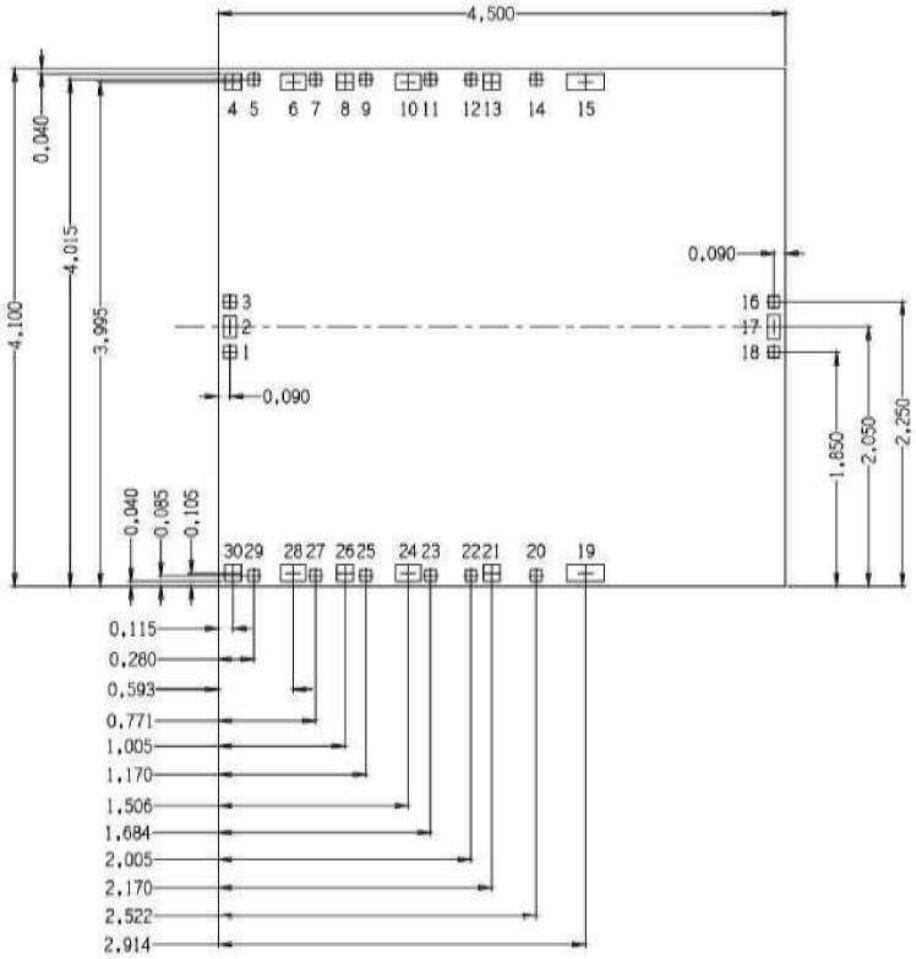
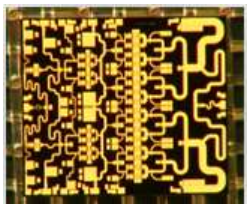


Figure 7 : Pad layout drawing

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50036-AC-AA** MMIC.



VWA-50042-AA

8 to 12 GHz – 25 dB – 12W
High Power Amplifier MMIC

Description

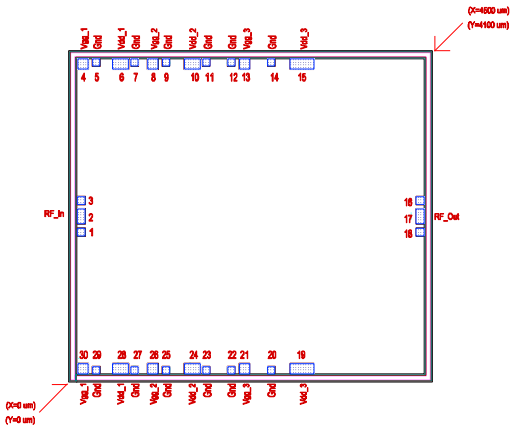
The **VWA-50042-AA** is a 3 Stages analog High power MMIC amplifier operating in the frequency range 8 to 12 GHz.

The device is a cascaded 3 stages amplifier designed in 0.25µm pHEMT process.

The devices is capable of more than +41 dBm output power at P sat, and provide more than 25dB of large signal gain from 8 to 12 GHz with less than 1 dB of Gain variation. The Design has been optimized to provide high efficiency, supply current is as low as 4,5 A with VD=+8,5V, when delivering +41 dBm output power.

S2P file can be provided for system design simulation.

GDSII file is also available for mechanical design.



Pin out and dimensions
(4,5 X 3,9 X 0.10 mm)

Features

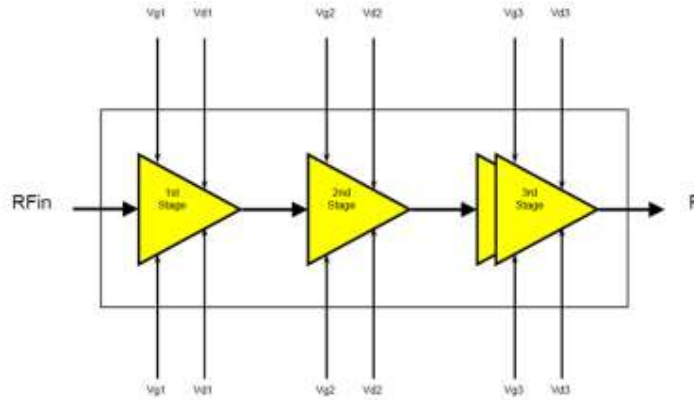
- 3 stages High Power pHEMT GaAs MMIC
- Wide band : 8 to 12 GHz
- High Output Psat > +41 dBm
- High P1dB > + 40dBm
- High large signal gain: 25dB min
- 50Ω, AC coupled RF input and output,
- Power supply: 4,5 A @ +8,5 V; Vg=-0,7 V
- 4,5 x 3,9 x 0.10 mm

Applications

- X band High Power amplifier
- Broadband communication
- Radar
- Test and measurement

Ordering information

Product code
VWA 50042 AA, Die
VWA 50042 AA, on carrier
VWA 50042 AA, on carrier, with power supply



Functional Block Diagram

Typical Characteristics: Tamb = 25°C, VD = +8,5V, ID = 4,5A (ID1N=ID1S=150 mA, ID2N=ID2S=400mA, ID3N=ID3S=1,4A), measured in pulsed mode for F= 10 KHz and duty cycle 10%.

Parameter measured in pulse mode	Symbol	Min	Typ	Max	Unit
Frequency range	F	8		12	GHz
Gain from 8 to 12 GHz	G		25		dB
Gain flatness from 8 to 12 GHz	ΔG		+/- 0,7		dB
Noise figure @ 10 GHz	NF		TBD		dB
Input adaptation from 8 to 12 GHz	S11		12		dB
Output adaptation from 8 to 12 GHz	S22		12		dB
Output power @ 1dB compression	P1dB		40		dBm
Saturated output power	PSat		41		dBm
Operating Drain supply voltage	VD	8		8,5	V
Supply current total	ID		4,5		A

Measurement reference planes are the INPUT and OUTPUT plans of the Die.

Environment Parameters	Symbols	Min	Max	Units
Storage temperature	Tst	-55	+85	°C
Operating temperature	Top	-40	+85	°C

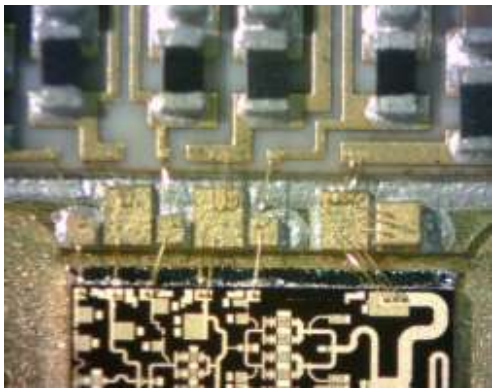
Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Drain Voltage	VD		9	V
RF input power (In)	Pin max		+23	dBm
Temperature process max 20 secondes	T process		325	°C

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

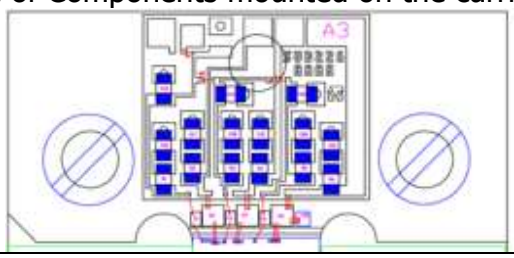
Application circuit:

Die mounted on carrier

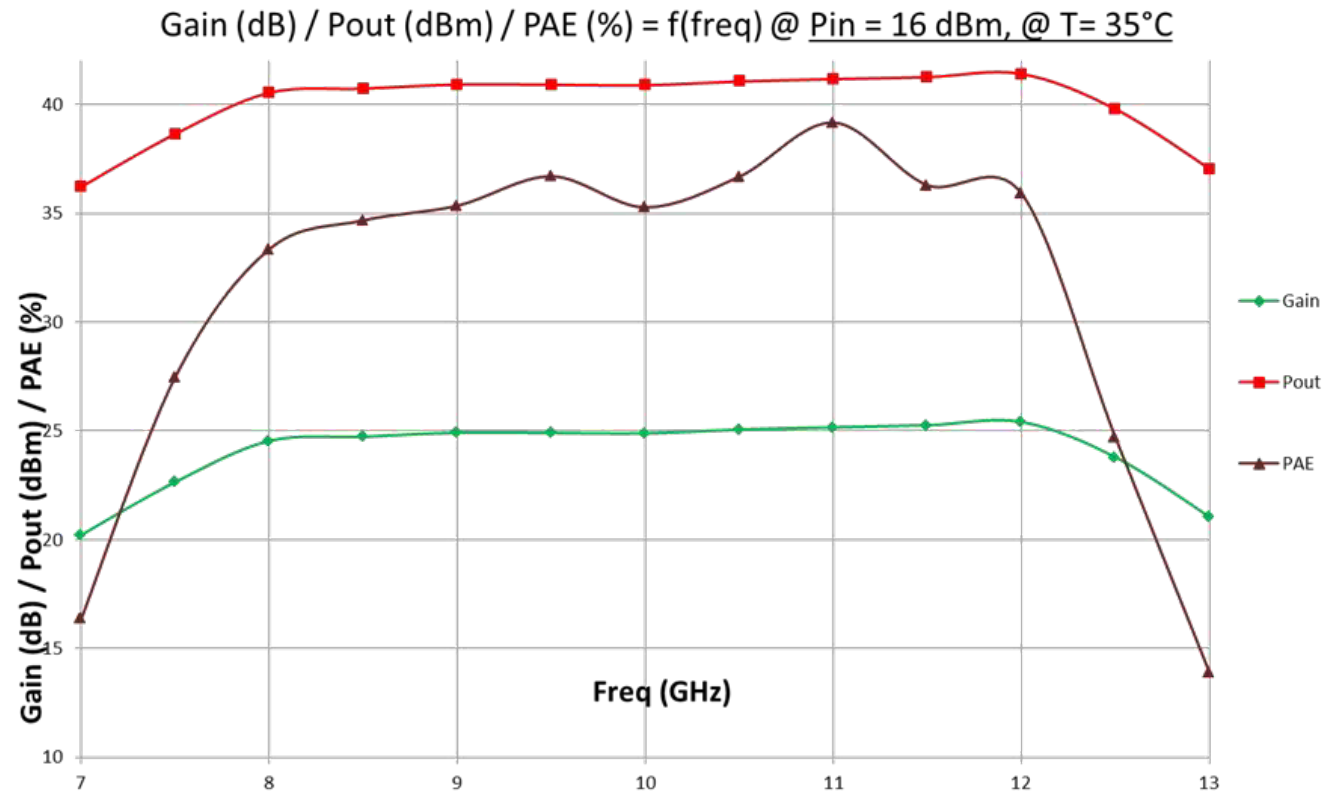


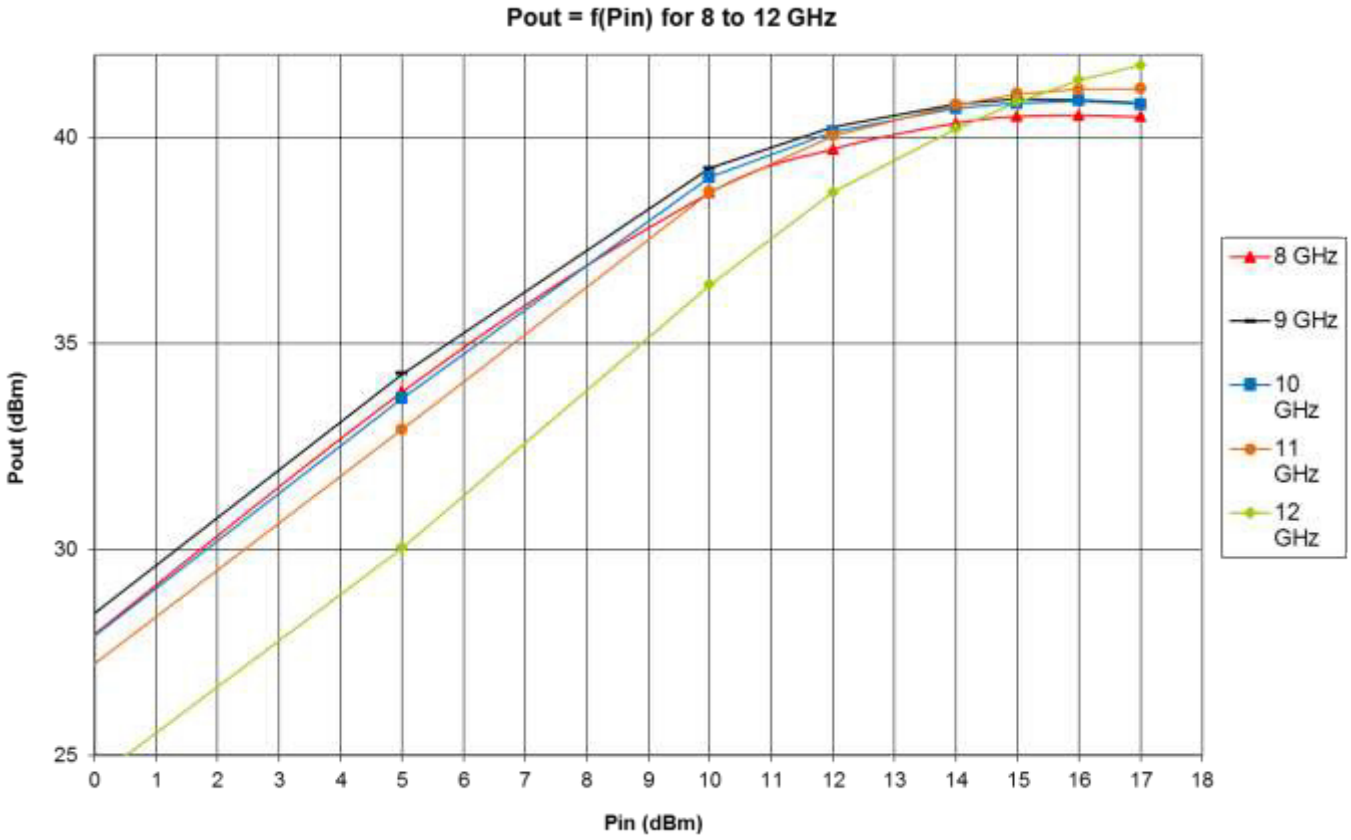
150pF	C1 C3 C5 C7 C9 C11
100pF	C2 C4 C6 C8 C10 C12
10nF	C16 C18 C20 C25 C27 C29
220nF	C17 C19 C21 C26 C28 C30
10nF	C31 C32
1µF	C13 C14 C15 C22 C23 C24
0Ω	R1 R3 R5 R7 R9 R11
11Ω	R2 R4 R6 R8 R10 R12

Table of Components mounted on the carrier



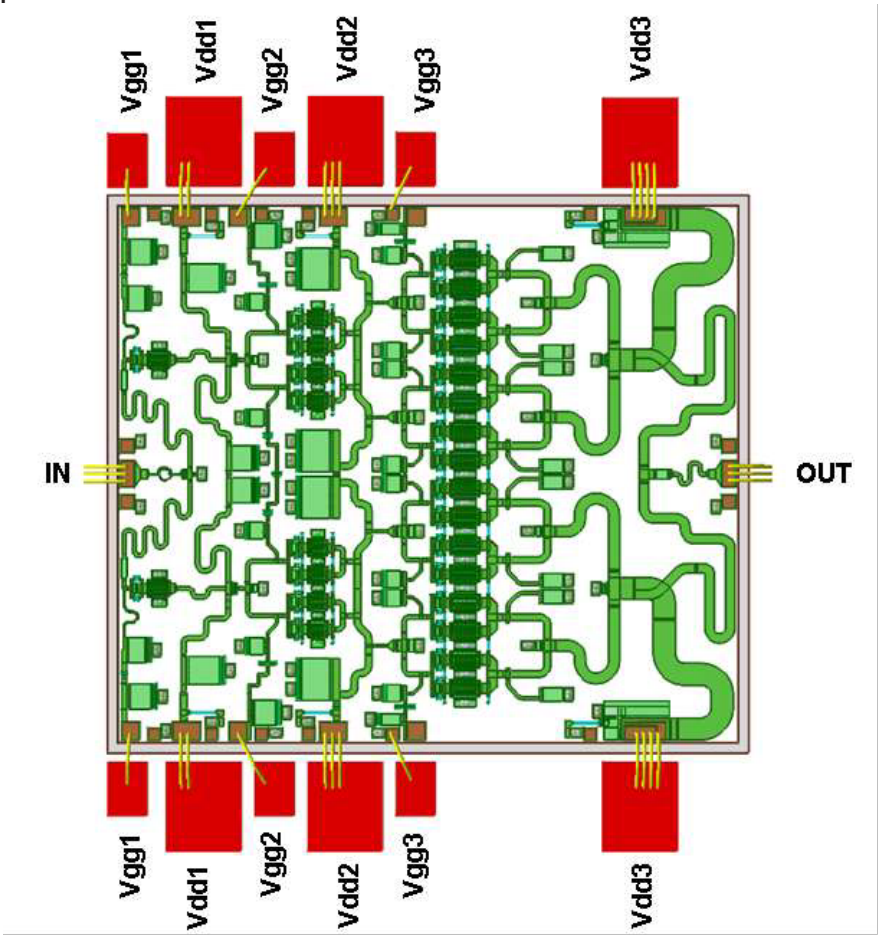
Typical test results in pulse mode





Die Lay out

The Die is symetrical on the RF axis. The die positionned top view with RF input on the left and RF output on the right show DC accesses on the top labelled north (N) and DC accesses on the bottom labelled south (S). VD1N, VD2N, VD3N, VG1N, VG2N, VG3N are DC signals applied on the north side, VD1S, VD2S, VD3S, VG1S, VG2S, VG3S are DC signals applied on the south side. Many ground accesses are complementing the pad layout. The backside is the ground reference plan.



Pin Out

The amplifier has a North face and a south face, north is top and south is bottom when RF input is on the left an RF output on the right.

Symbol	Pad	Description
RFOUT	OUT	RF output
RFIN	IN	RF input
VD1N	VD1N	First stage Drain (amplifier North)
VD2N	VD2N	Second stage Drain (amplifier North)
VD3N	VD3N	Third stage Drain (amplifier North)
VG1N	VG1N	First stage Gate (amplifier North)
VG2N	VG2N	Second stage Gate (amplifier North)

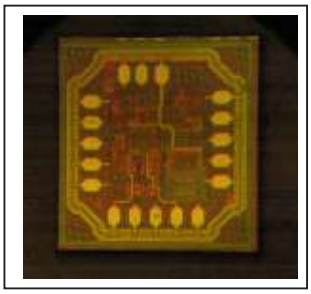
VG3N	VG3N	Third stage Gate (amplifier North)
VD1S	VD1S	First stage Drain (amplifier South)
VD2S	VD2S	Second stage Drain (amplifier South)
VD3S	VD3S	Third stage Drain (amplifier South)
VG1S	VG1S	First stage Gate (amplifier South)
VG2S	VG2S	Second stage Gate (amplifier South)
VG3S	VG3S	Third stage Gate (amplifier South)
GND	BACKSIDE	Ground

Bonding Pad Coordinates

Pad	X (um)	Y (um)	Size (um x um)	Function
1	90	1780	100 x 100	Gnd
2	90	1980	100 x 190	RF_IN
3	90	2180	100 x 100	Gnd
4	150	3810	130X130	Vgg1_A
5	315	3810	90X90	Gnd
6	620	3810	200X130	Vdd1_A
7	800	3810	90X90	Gnd
8	1035	3810	130X130	Vgg2_A
9	1200	3810	90X90	Gnd
10	1530	3810	200X130	Vdd2_A
11	1710	3810	90X90	Gnd
12	2030	3810	90X90	Gnd
13	2200	3810	130X130	Vgg3_A
14	2530	3810	90X90	Gnd

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50042-AA** MMIC.



NRZ to RZ DPSK
VWA-28-NRZtoRZ_DPSK-SD

10 – 28 Gb/s

Description

The **VWA 50001 AA** chip is a NRZ to RZ DPSK coder for high data rate application, typically 10 to 28 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (DFF_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is synchronized by the input clock and electrically coded to the RZ DPSK format. The output is a 3 level signal: positive and negative pulses are generated to the output, according to the clock rate. A RZ coding is applied on the top of a differential coding: for a "1" present to the input, the output pulse sign changes at every clock transition and for a "0" the pulse sign remains the same.

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Single MZ modulator NRZ to RZ DPSK coding
- Fiber transmission

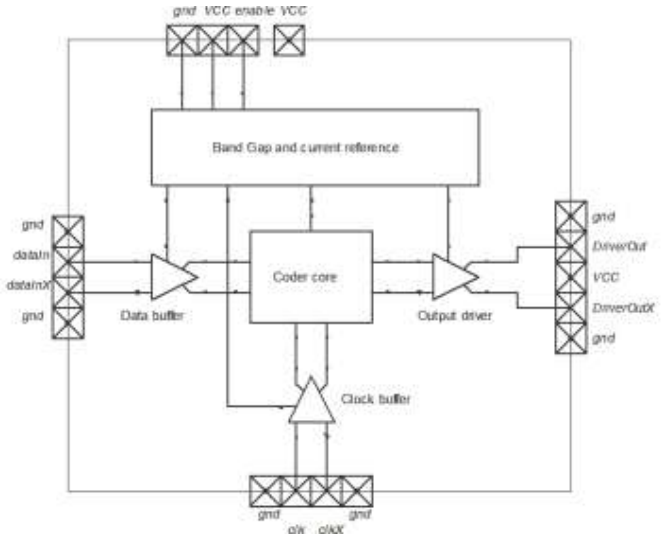
Ordering information

Part Number: VWA 50001 AA

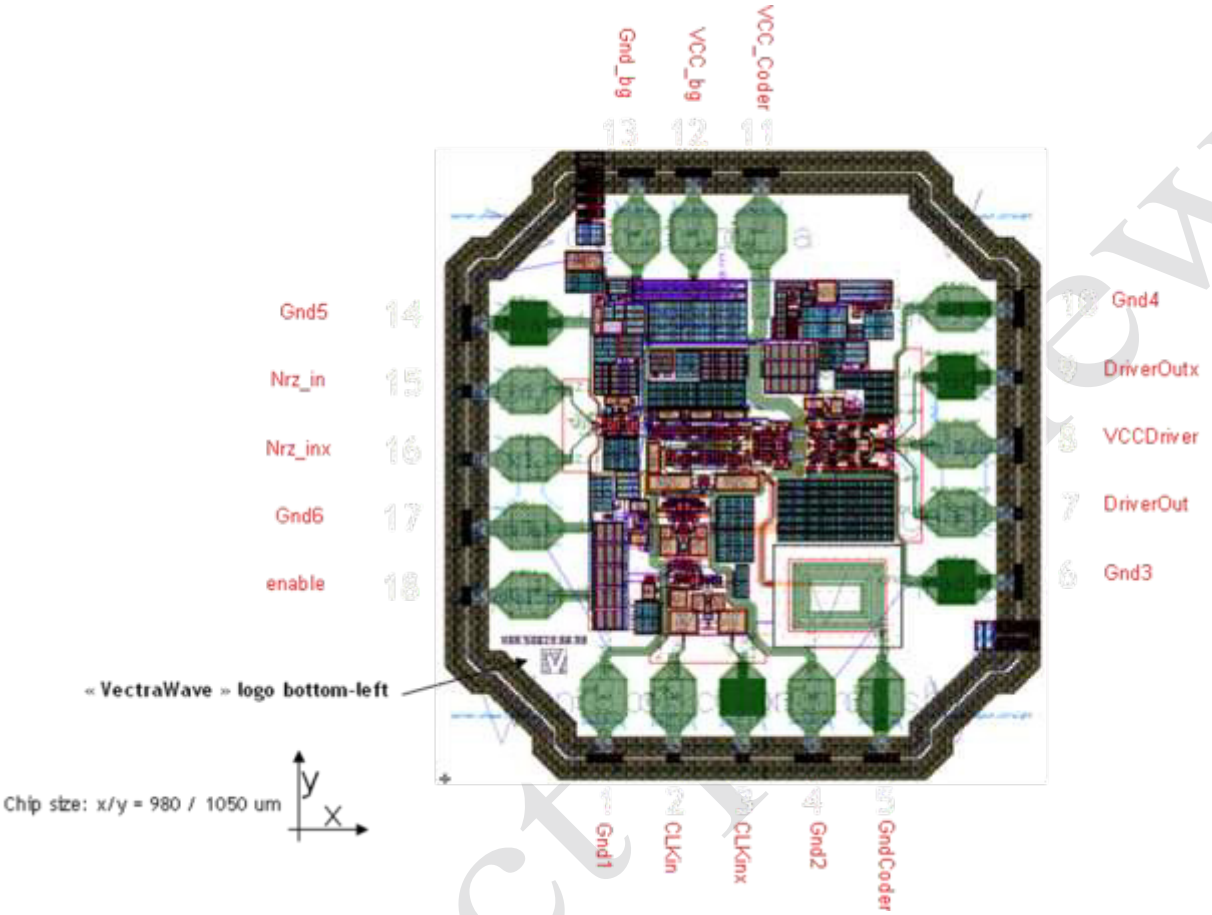
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 25Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.

VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
		Chip bias				
Supply voltage	VccCoder – VccBG	Vcc		3		V
	VccDriver		2.5	3	4	V
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		nA
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	uA
	VccDriver; enable=0; T=27°C	VccDriver0		27		pA
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		20		mA
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	mA
	VccDriver; enable=1	VccDriver1		160		mA
		Data input (Nrz_in and Nrz_inx)				
Input impedance	Single and differential modes	Zin		100		Ω
Amplitude range**	Single or differential input		2	300		mVpp
		Clock input (Clkin and Clkinx)				
Input impedance	Single and differential modes			100		Ω
Amplitude range**	Single or differential input		1	300		mVpp
Frequency range***					25	GHz
Phase margin				Tbit/4		
		Driver Output				

Output impedance	**Single / Differential**			50 / 100		**Ω**
Common mode voltage	**Referred to VCCDriver**			VCCDriver-0.350		**V**
Amplitude	**Single**			400		**mVpp**

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG - VccDriver**	**Vcc**	-0.5		4.6	**V**
Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

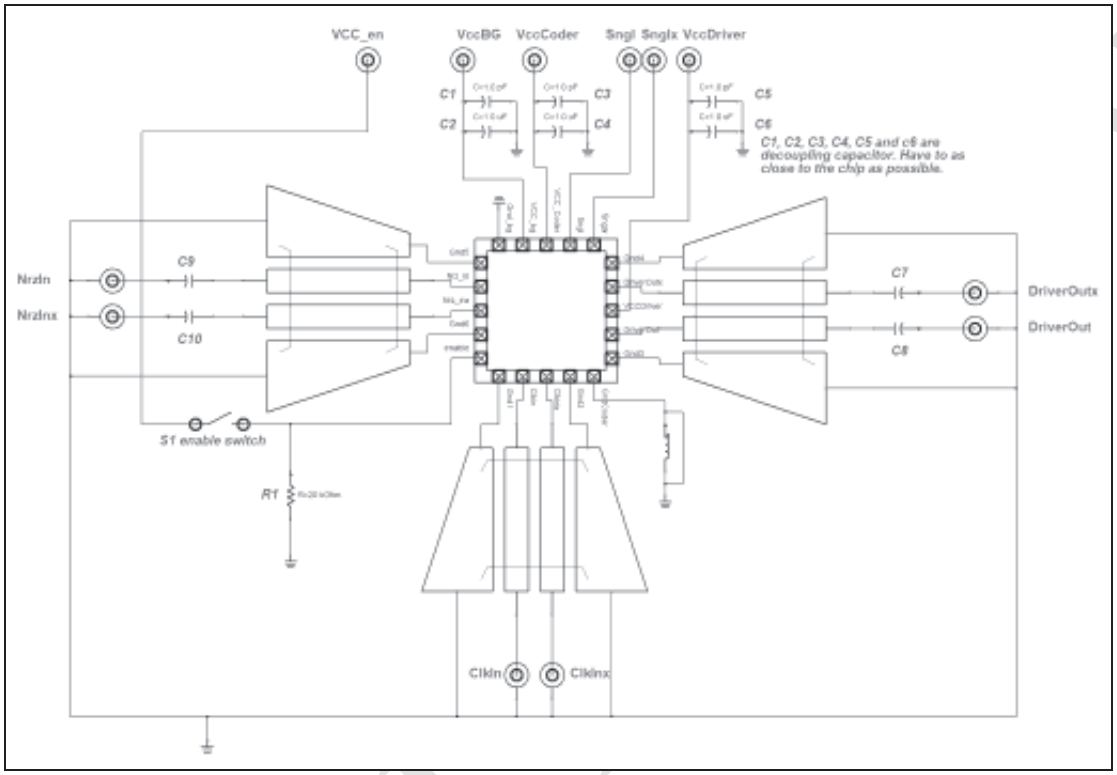
ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

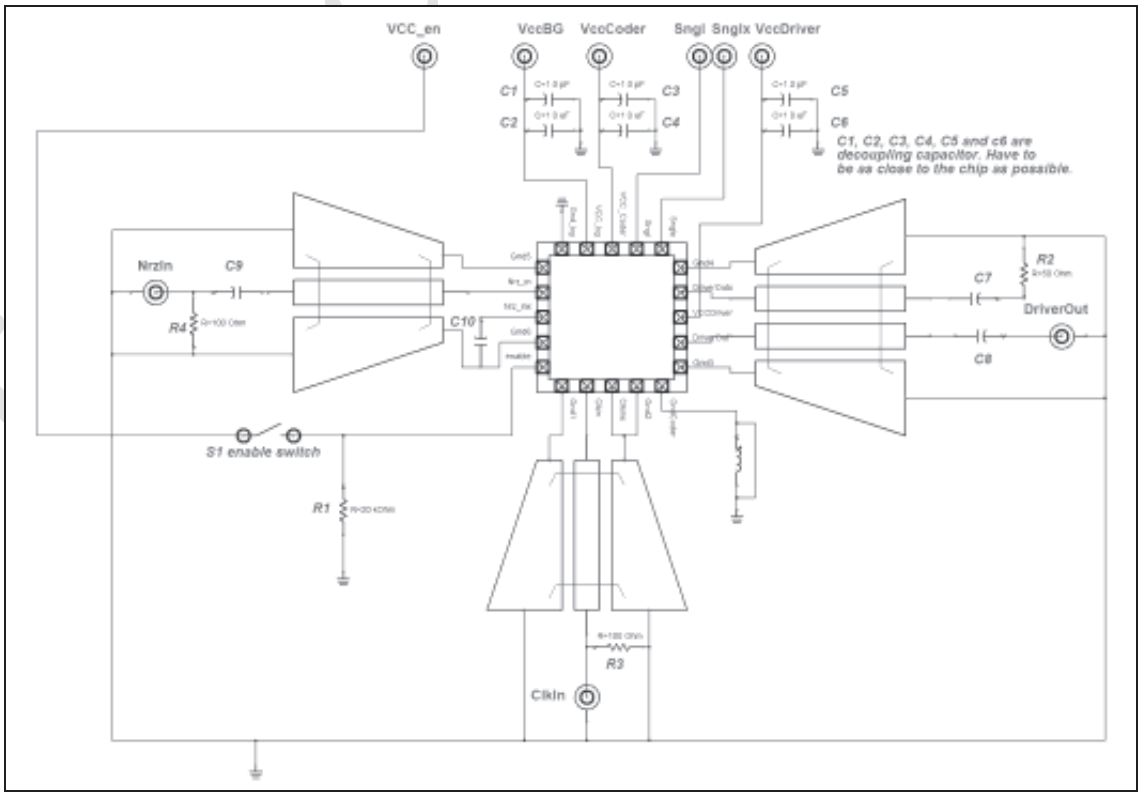
*Human Body Model

Application schematic

Differential IN and OUT



Single-ended IN and OUT



Output characteristics - simulated

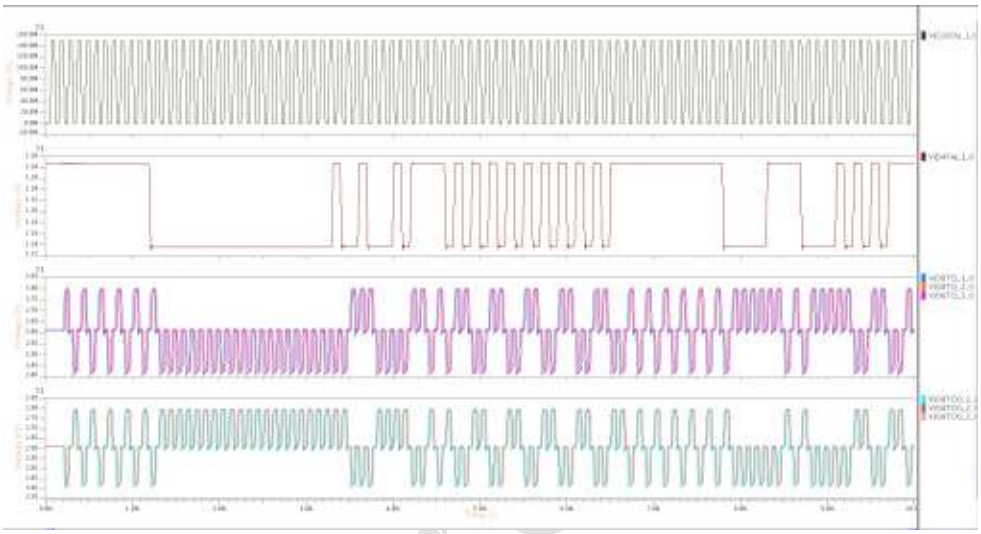
Typical coder response: for -40 (_1), 27 (_2) and 100 (_3)°C

Clock:
Frequency = 10 GHz
Amplitude = 150 mVpp

Signal:
Data rate = 10 Gb/s - NRZ
Amplitude = 150 mVpp

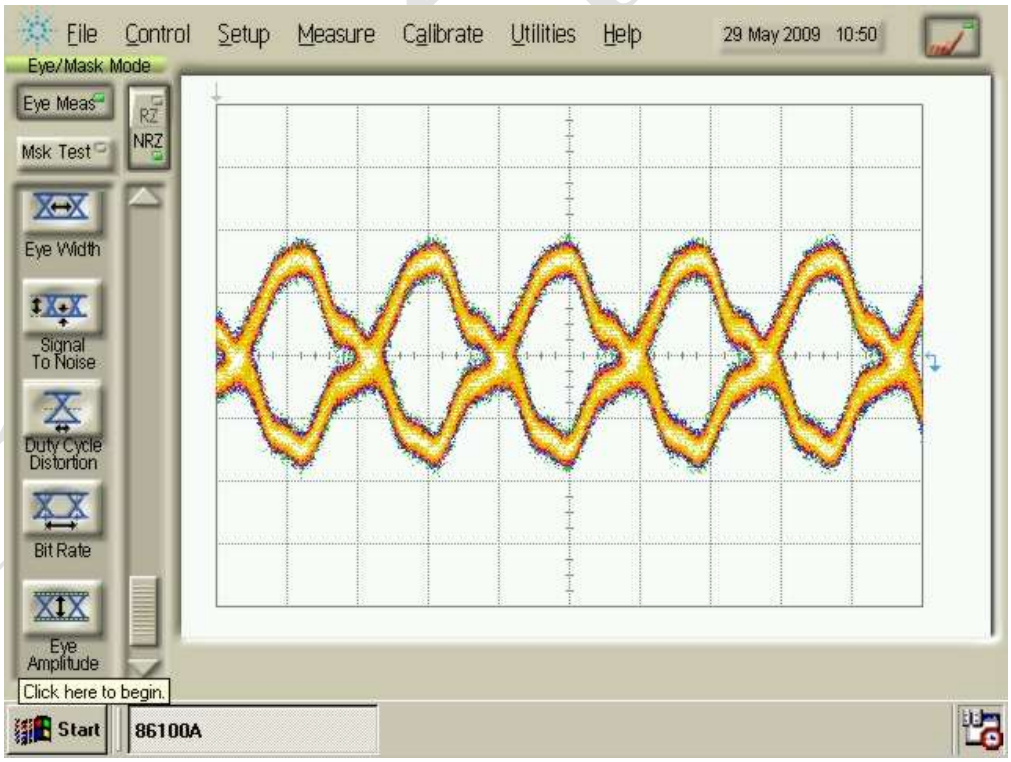
Driver0ut: 50Ω loaded

Driver0utx: 50Ω loaded

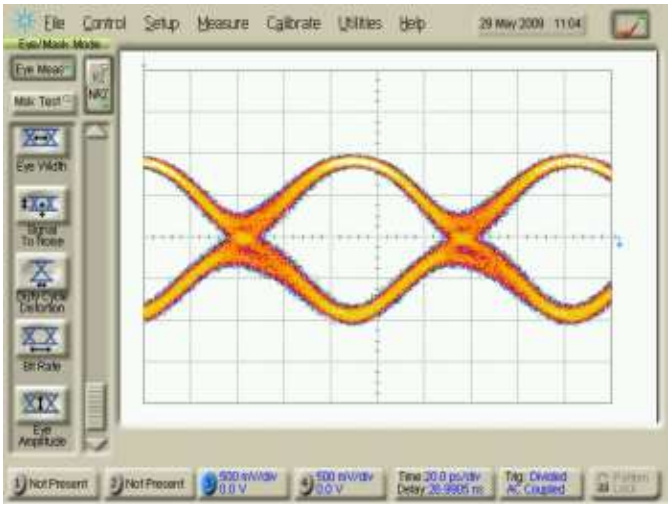


Eye diagram measurement @12.5Gbps

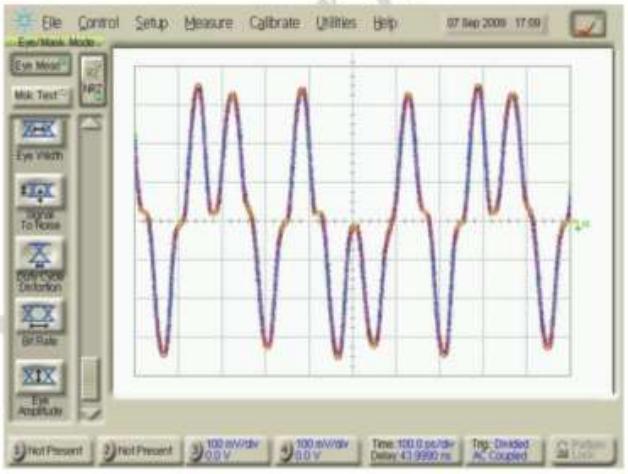
Measurement conditions: single-ended IN and OUT, measured directly to the chip output



Measurement conditions: single-ended IN and OUT, measured after driver:



Output signal - measurement

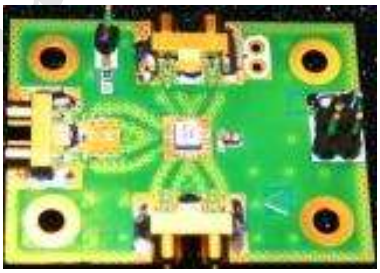


Differential output (QFN package) @12.5Gbps

Ordering information :

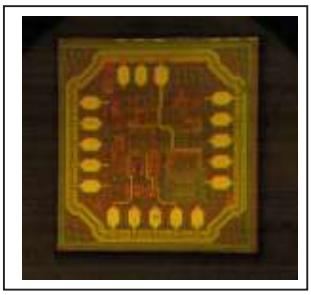
Product number	Package type	Function	Min Qty order
VWA 50001 AA	Die	NRZ to RZ_DPSK	10
VWA 00055 AA	QFN 3X3	NRZ to RZ_DPSK	5
VWA 00077 AB	GPPO QFN Evaluation board	NRZ to RZ_DPSK	1
VWA 00068 AB	6 K connector package	NRZ to RZ_DPSK	1

VWA Packaged Form Proposition



Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.



D Flip Flop
VWA-40-DFF-SD

10 – 40 Gb/s

Description

The **VWA 50002 AA** chip is a D Flip Flop for high data rate application, typically 10 to 40 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (DFF_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is transferred to the output for each clock rising edge. The output amplitude is 400 mV pp single ended (800 mV differential pp).

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Data synchronization
- Fiber transmission

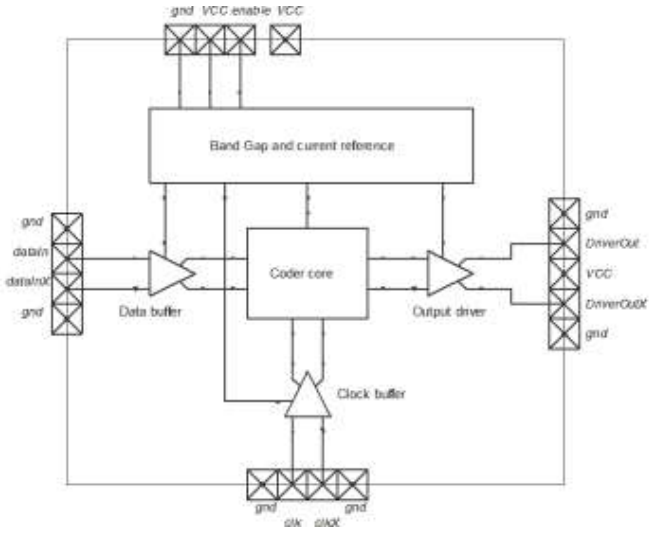
Ordering information

Part Number: VWA 50002 AA

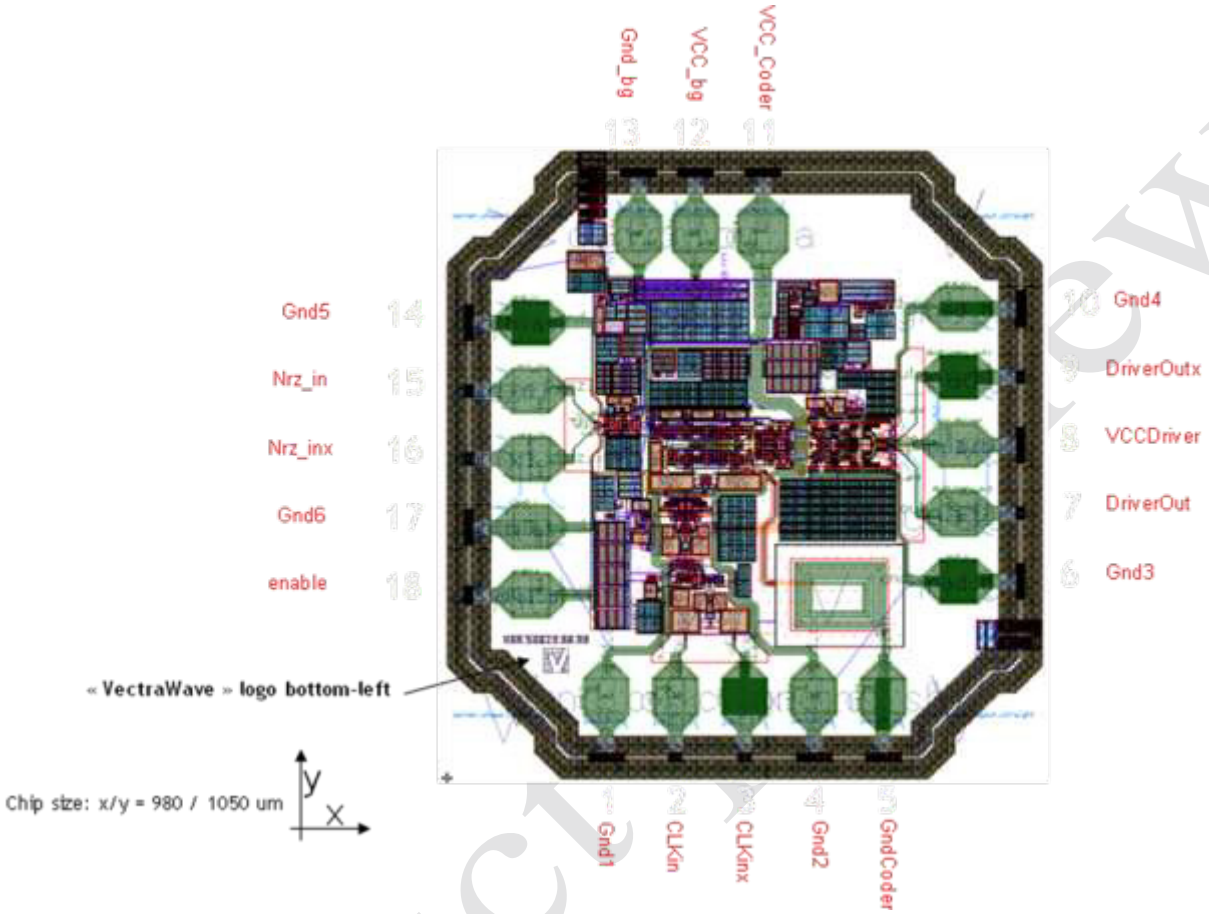
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 25Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if

		not used.
VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Chip bias						
Supply voltage	**VccCoder – VccBG**	**Vcc**		3		**V**
	VccDriver		2.5	3	4	**V**
Current consumption OFF mode*	**VccCoder; enable=0; T=27°C**	**VccCoder0**		3		**nA**
	VccBG; enable=0; T=27°C	**VccBG0**	(100°C) 0.01	15	(-40°C) 28	**uA**

	VccDriver; enable=0; T=27°C	**VccDriver0**		27		**pA**
Current consumption ON mode*	**VccCoder; enable=1**	**VccCoder1**		125		**mA**
	VccBG; enable=1	**VccBG1**	(-40°C) 2		(100°C) 2.5	**mA**
	VccDriver; enable=1	**VccDriver1**		16		**mA**
Data input (Nrz_in and Nrz_inx)						
Input impedance	**Single and differential modes**	**Zin**		100		**Ω**
Amplitude range**	**Single or differential input**		2	300		**mVpp**
Clock input (Clkin and Clkinx)						
Input impedance	**Single and differential modes**			100		**Ω**
Amplitude range**	**Single or differential input**		1	300		**mVpp**
Frequency range***					25	**GHz**
Phase margin				Tbit/4		
Driver Output						
Output impedance	**Single / Differential**			50 / 100		**Ω**
Common mode voltage	**Referred to VCCDriver**			VCCDriver-0.350		**V**
Amplitude	**Single**			400		**mVpp**

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG -**	**Vcc**	-0.5		4.6	**V**

	VccDriver					
Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

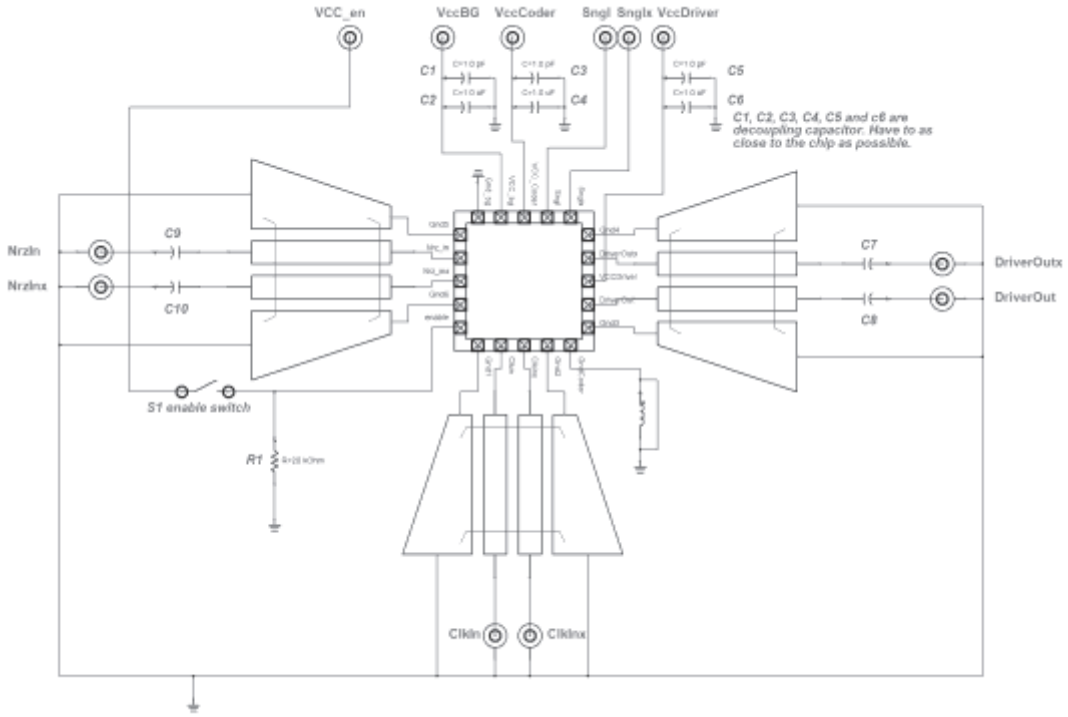
ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

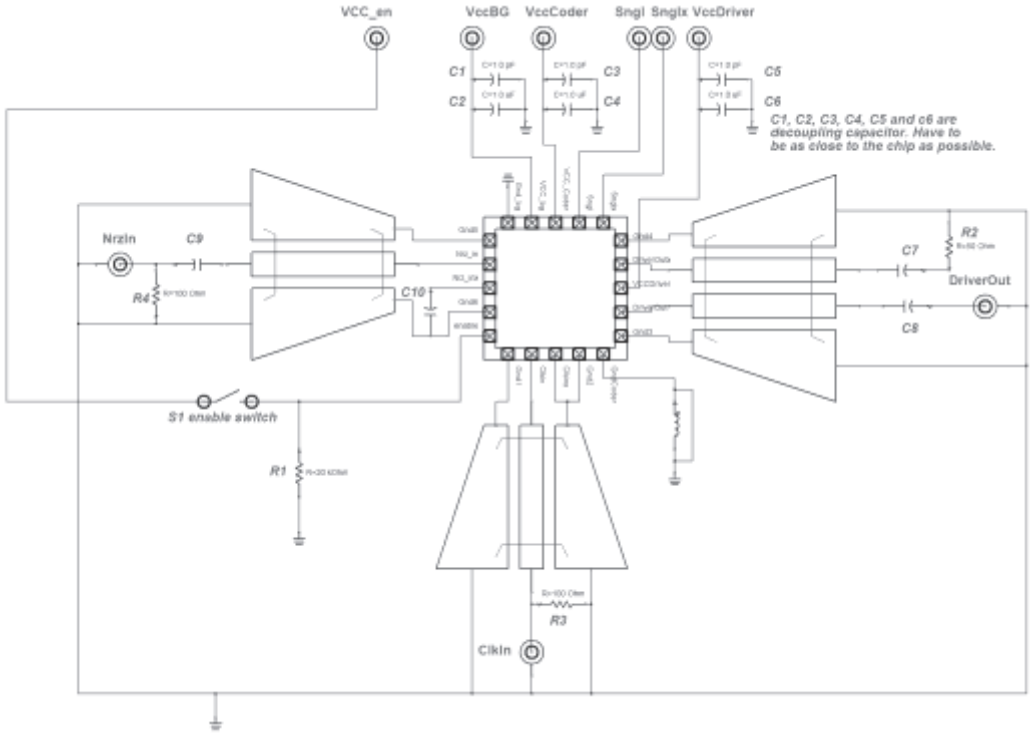
*Human Body Model

Application schematic

Differential IN and OUT



Single-ended IN and OUT



Output characteristics - simulated

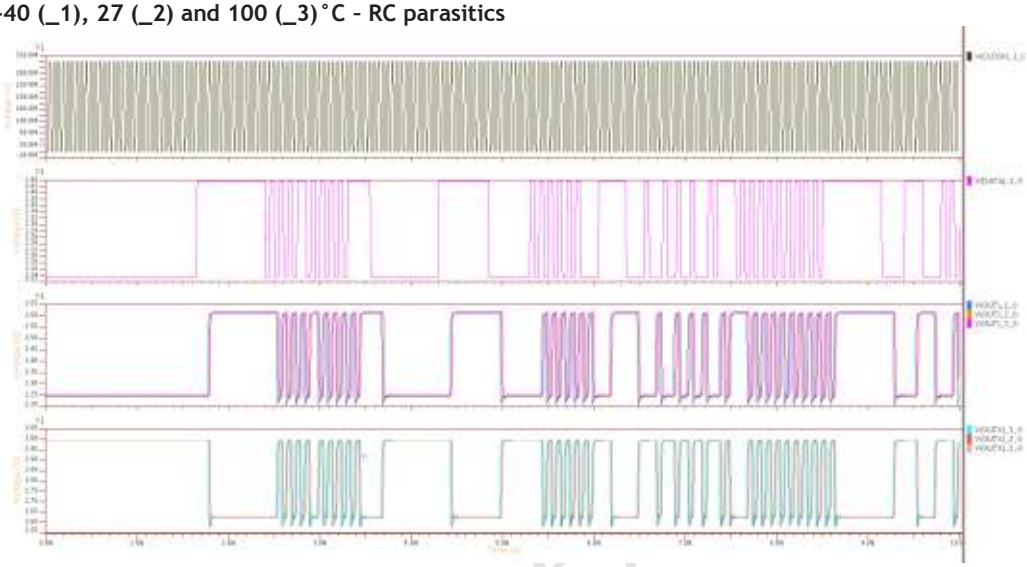
Typical coder response: for -40 (_1), 27 (_2) and 100 (_3)°C - RC parasitics

Clock:
Frequency = 20 GHz
Amplitude = 300 mVpp

Signal:
Data rate = 20 Gb/s - NRZ
Amplitude = 300 mVpp

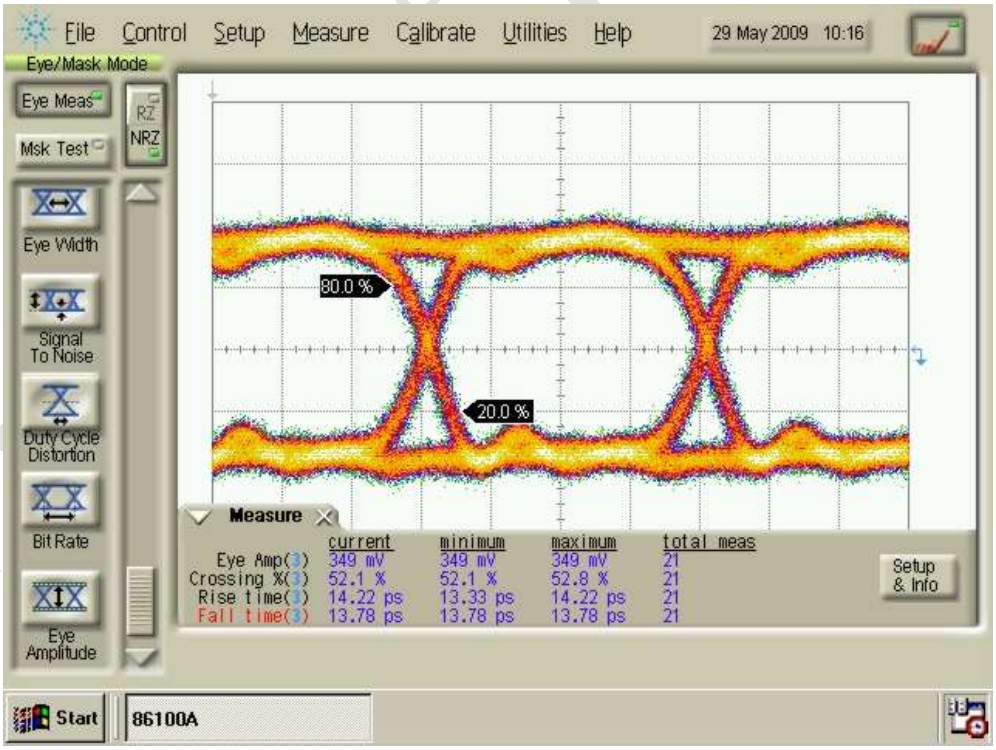
Driver0ut: 50Ω loaded

Driver0utx: 50Ω loaded



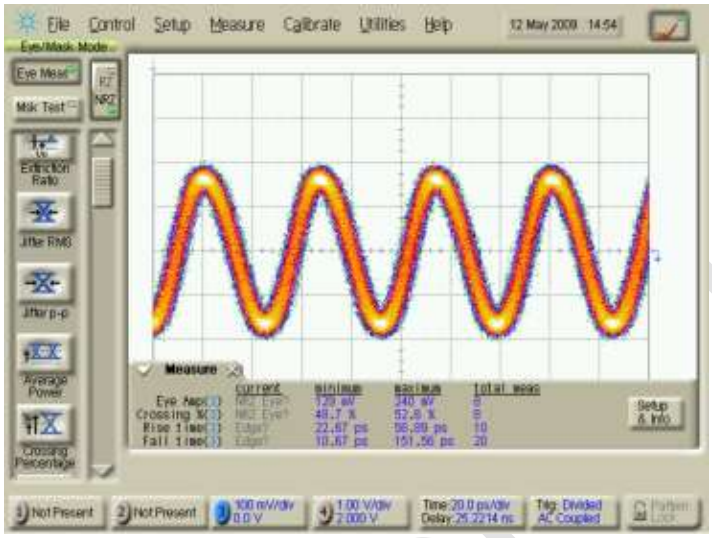
Eye diagram measurement @12.5Gbps

Measurement conditions: single-ended IN and OUT, measured directly to the chip output



VWA 00069 AB (6K Housing) Eye diagram measurement @43Gbps

Measurement conditions: single-ended IN and OUT, measured directly to the chip output.
The "Signal Input" is a 21.5 GHz harmonic signal (representing a continuous 10101 series).
The "Clock Input" is a 43.5 GHz harmonic signal.



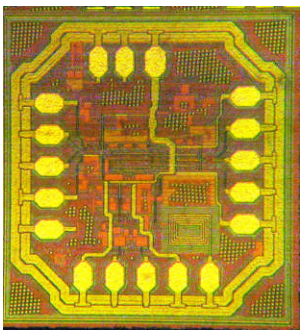
Ordering information :

Product number	Package type	Function	Min Qty order
VWA 50002 AA	Die	DFF	10
VWA 00056 AA	QFN 3X3	DFF	5
VWA 00088 AB	GPPO QFN Evaluation board	DFF	1
VWA 00069 AB	6 K connector package	DFF	1

VWA Packaged Form Proposition

Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.



VWA-50011 AA

Power Controller for high data rate application

Description

The **VWA-50011 AA** is a power controller for high data rate application. it is used into the TX modules that are used to drive the data to the MZ $LiNbO_3$ optical modulator. This type of device requires a drive voltage of about 8 to 10V typically that has to be continuously monitored and controlled. *The controller has been developed with the Jazz SBC18 process, using its high speed HBT option in order to integrate the detector on chip. Therefore, the chip can directly be used into a module as GaAs PA companion with no additional diode detector.*

For this type of application, the PA or data driver is generally a GaAs distributed amplifier 100 KHz to 15 GHz for a 10 Gbits/s application. Its output level is coupled to the detector input in order to ensure a level of about 1 Vpp. The controller input stage is a peak detector, linear in linear (means that the detector output level is proportional to the amplitude of the signal and not to the power in dBm).

The power control principle consists in comparing the detected power value to an external wanted (set) value; the control loop modifies the PA gain / power control DC voltage value in order to match the wanted value to the set value. If a voltage ramp is applied to the set value, the PA output amplitude increases linearly.

The specification is closely linked to the high data rate application, where there is no need for a high control dynamic range, but for an accurate output level control. *The detector is very application-specific: this is truly the part that has to be redesigned accordingly to the frequency, the dynamic and the process. The main part, which is the controller core, has been designed in CMOS. It is a design platform which is used into our controller family. The specifications can be modified upon customer's requests.*

Features

- Temperature and process compensated
- Dynamic range: linear from 0.2 to 1 Vp (no damage): single ended input.
- 2.9 to 3.3V voltage supply.
- Setting value from 0.3 to 1.8V full scale.
- External 50Ω resistor to the match the detector input
- External capacitor for feedback loop stabilization.

Advantages

The level control using the VWA 50011 AA does not have to be at "system level" as it is classically done.

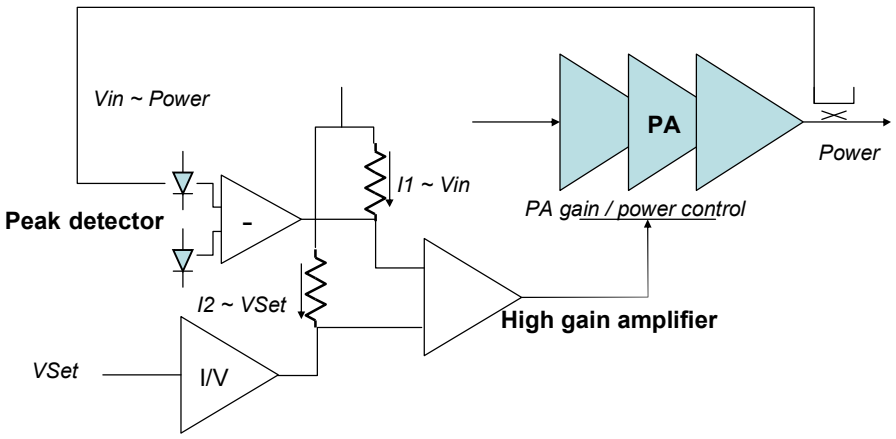
The controller includes a peak detector which is internally compensated (temperature and process). The output level is only linked to the Set Value, applied to the controller, independently of (Output-Level) VS (Gain / Level-Control) driver characteristics.

The driver characteristics dispersion (process) and variation (temperature and aging) are compensated by the control loop. A calibration at system level is no longer required.

Applications

- OC192-STM64-10GE long haul transmission
- SONNET –SDH optical systems
- Single MZ modulator solutions
- RZ DPSK coding

Simplified Functional Block Diagram



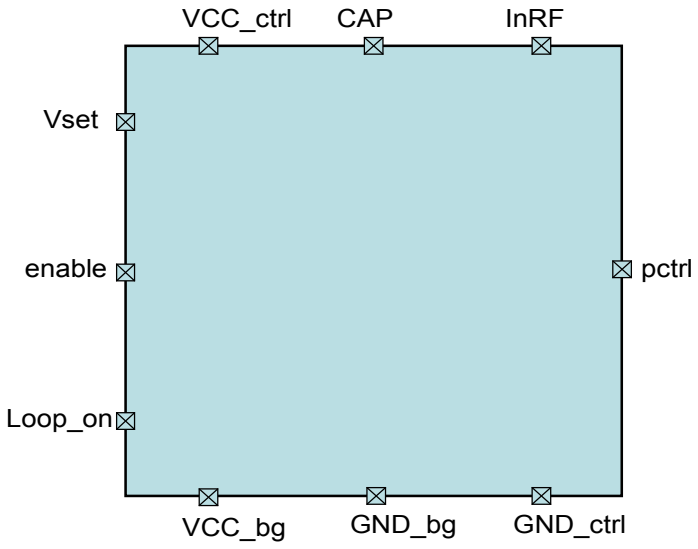
A part of the signal to the driver (PA) output is coupled to the peak detector. It uses two equivalent devices, one being used as reference. The actual signal level is the difference between the detected signal and the reference. The detected signal level is compared to the wanted value VSet and a High gain amplifier is used to close the loop. The signal to the High gain amplifier output, which control the driver level, is such that Vin ~VSet.

A scalling and offset can be done thanks to the use of the gm (I/V) device, loaded by a resistor depending on specific needs t is possible to have Vin (Driver Output Level) = α x VSet + β.
For the WVA 50011 AA, α ~ 2, β = 0

Pad list and description

Pad number	Pad Name	Description
1	VCC_bg	POWER supply for the internal voltage / current reference generator.
2	Gnd_bg	Voltage / current generator GROUND
3	Gnd_ctrl	Main controller (including the detector) ground
4	pctrl	ANALOG output: sets the PA gain level according the setting level (vset)
5	InRF	RF detector input
6	CAP	ANALOG input / output: stabilization capacitor
7	VCC_ctrl	POWER supply for the main controller part
8	vset	ANALOG input. Driver level setting value
9	enable	DIGITAL: set the chip ON = 1 / OFF = 0
10	Loop_on	DIGITAL: opens the loop = 0 / closes the loop = 1 If Loop_on = 0, pctrl stays unchanged independently to vset and InRF.

Chip pad-out



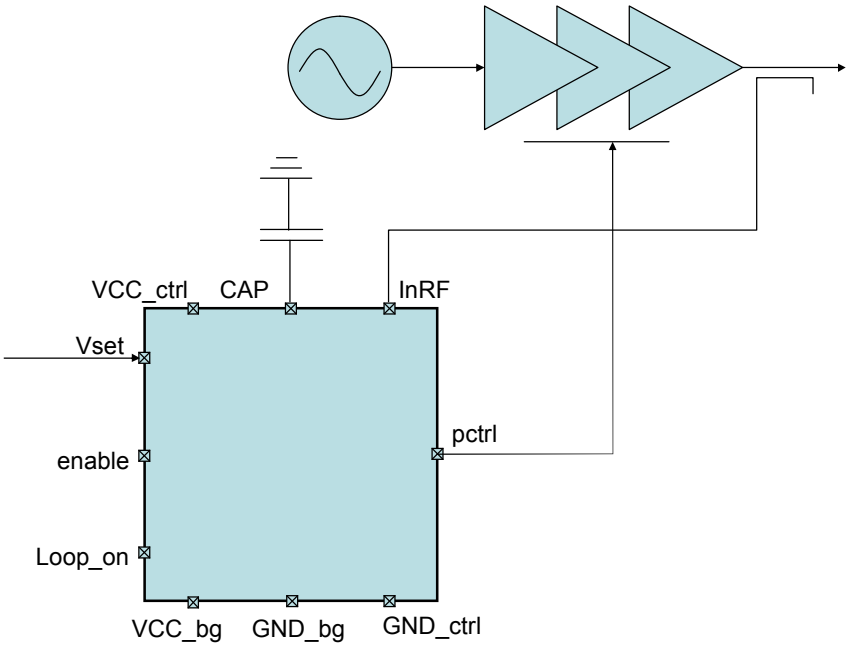
Measurement setup:

Nominal operation

For a nominal operation condition with a given VSET, the control loop is:

- **InRF** – peak detector – high gain stage – gain control buffer – **pctrl**

The PA output is coupled to the controller input **InRF**. The signal to InRF input has to be in the 0.2 to 1Vp range. The PA output level is controlled by the pad **pctrl** connected to the PA gain / power control pin. An external capacitor (typically uF) has to be connected to **CAP** to stabilize the loop. The value required depends on the PA (Pout VS gain control) transfer function.



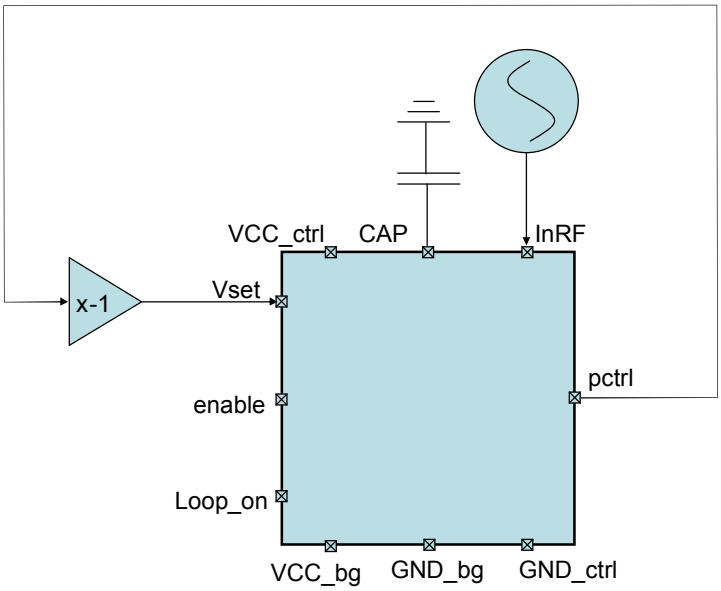
Power control characterization

The setup used to characterize the controller itself is slightly different to the previous one. The power source is directly applied to the controller RF input (InRF) and then the control loop is:

- Vset – gm amplifier - high gain stage – gain control buffer – **pctrl – (x-1)**

An external inverter is required (x-1) to add 180° phase into the loop and ensure the stability. As the loop is not designed to be used this way, additional decoupling capacitors may be required as well.

In the test condition reference PA is no longer required


VCC_ctrl
CAP
InRF
x-1
Vset
pctrl
enable
Loop_on
VCC_bg
GND_bg
GND_ctrl

Overall Specification

Parameter	Conditions	Min	Typ	Max	Units
Power supply: VCC_ctrl and VCC_bg					
Supply Voltage	VCC	2.9		3.3	V
Supply Current*	Enable High		6	10	mA
Shutdown Supply Current	Enable Low			1	uA
InRF pad: detector input					
Frequency Range (peak detector)				30	GHz
RF input voltage range (linear range)		0.2		1	Vpp
Slope (VSet / VRF pp)	RF freq=10 GHz		1.8		
Intercept	RF freq=10 GHz		0		V
RF Input Resistance**			2		kOhm
RF Input Capacitance**			1		pF
Digital inputs: enable and Loop_on					
Logic Low				0.8	V
Logic High		1.8			V
VSET pad: setting value					
VSet Input Range		0.4		1.8	V
VSet slew rate			16		V/us
VSet Input Resistance (CMOS gate)		30			MOhm
pctrl pad: PA power control					
Output Voltage Range (PA power control)	Pctrl pin	0.2		VCC_ctrl – 0.2	V
Output Current			14		mA
Output Slew Rate	No Capacitor on Filter		20		V/uS
Output Buffer Noise			25		nV/√Hz
Die Size	TBC			0.980	mm^2

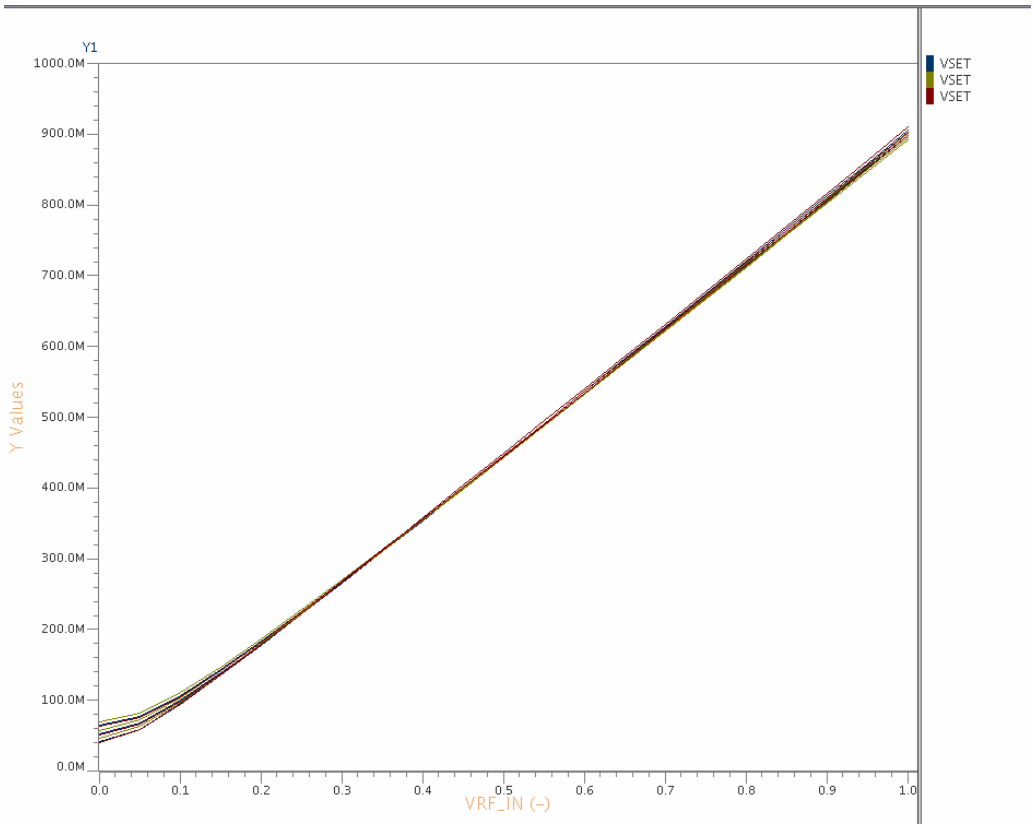
** Not including the current control to the PA*

*** The 50Ω matching is made with an external resistor*

On Chip Characteristics:

The following characteristics have been simulated using the "power control characterization" setup as previously described. The power source is directly connected to the detector input and the loop is closed between pctrl and VSET

The simulations have been made over process for -40, 27 and 100°C



Environment Parameters

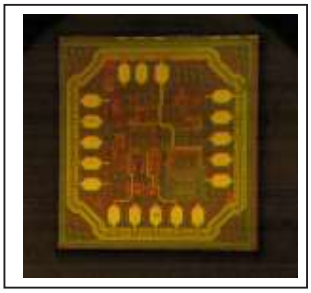
Maximum ratings	Symbols	Min	Typ	Max	Units
Operating temperature (case)	Top	-40		+100	°C

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50011 AA** chip.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

VWA 50023AAA DS Rev 0.4



Differential Coder
VWA-28-DIFF-SD

10 – 28 Gb/s

Description

The **VWA 500023 AA** chip is a NRZ differential coder for high data rate application, typically 10 to 28 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (DIff_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is synchronized by the clock and electrically coded to a differential format. If a logical zero is present to the input, the output remains unchanged: Qn+1=Qn. If a logical one is present to the data input, the output value is changed at every rising edge of the clock: a constant one to the input gives a continuous series of 01010 to the output.

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- NRZ to RZ DPSK data coding
- Fiber transmission

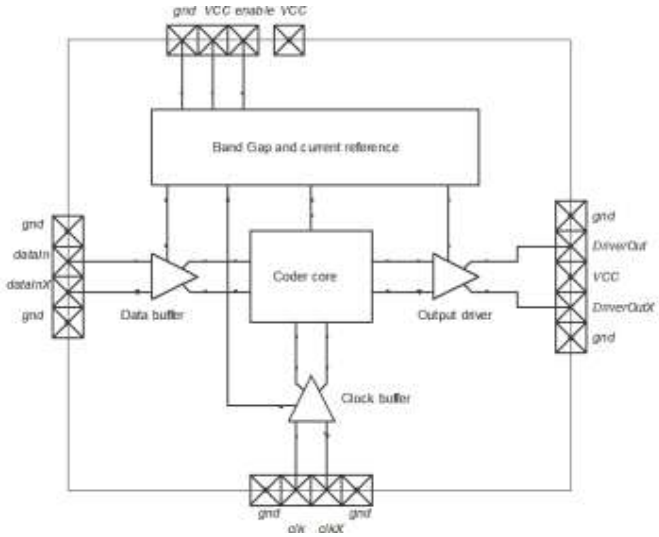
Ordering information

Part Number: VWA 500023 AA

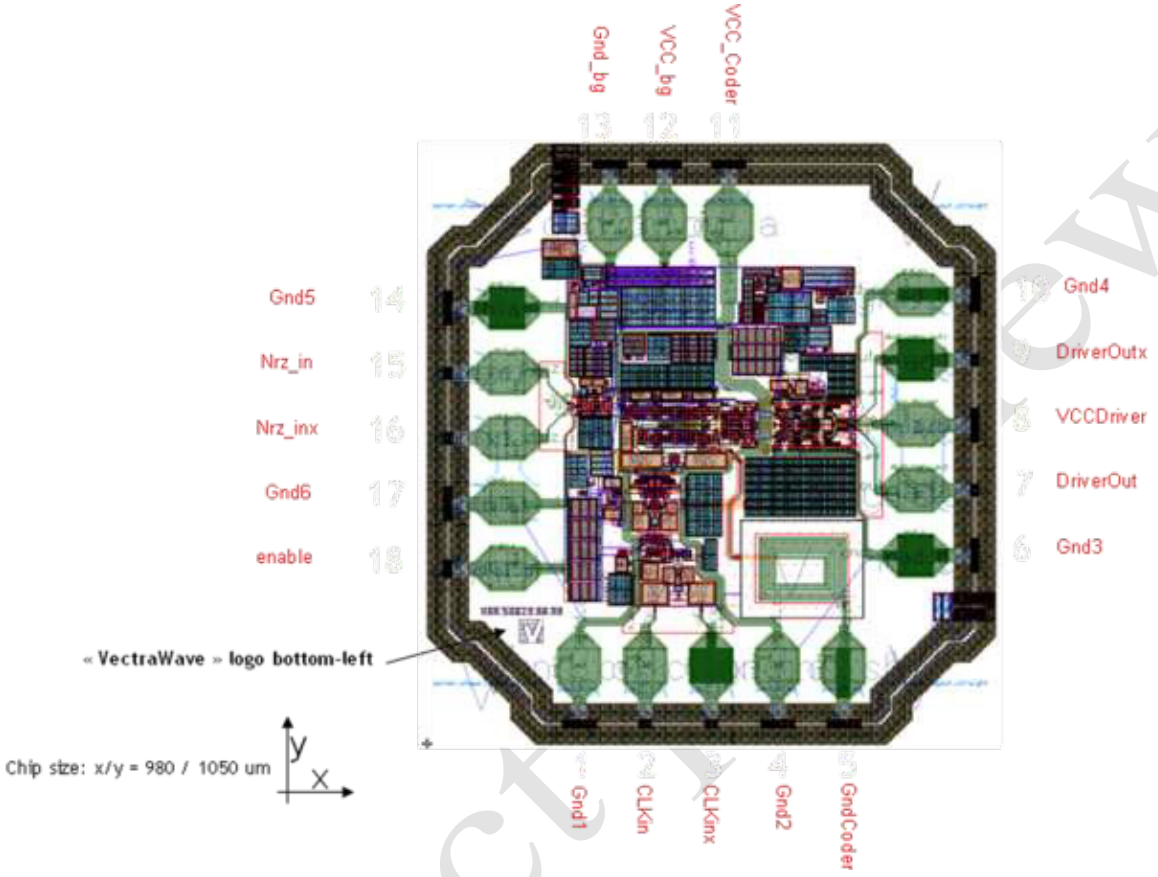
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 28Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.

VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
		Chip bias				
Supply voltage	VccCoder – VccBG	Vcc		3		V
	VccDriver		2.5	3	4	V
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		nA
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	uA
	VccDriver; enable=0; T=27°C	VccDriver0		27		pA
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		20		mA
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	mA
	VccDriver; enable=1	VccDriver1		150		mA
		Data input (Nrz_in and Nrz_inx)				
Input impedance	Single and differential modes	Zin		100		Ω
Amplitude range**	Single or differential input		2	300		mVpp
		Clock input (Clkin and Clkinx)				
Input impedance	Single and differential modes			100		Ω
Amplitude range**	Single or differential input		1	300		mVpp
Frequency range***					25	GHz
Phase margin				Tbit/4		

Driver Output						
Output impedance	**Single / Differential**			50 / 100		**Ω**
Common mode voltage	**Referred to VCCDriver**			VCCDriver-0.350		**V**
Amplitude	**Single**			400		**mVpp**

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG - VccDriver**	**Vcc**	-0.5		4.6	**V**
Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

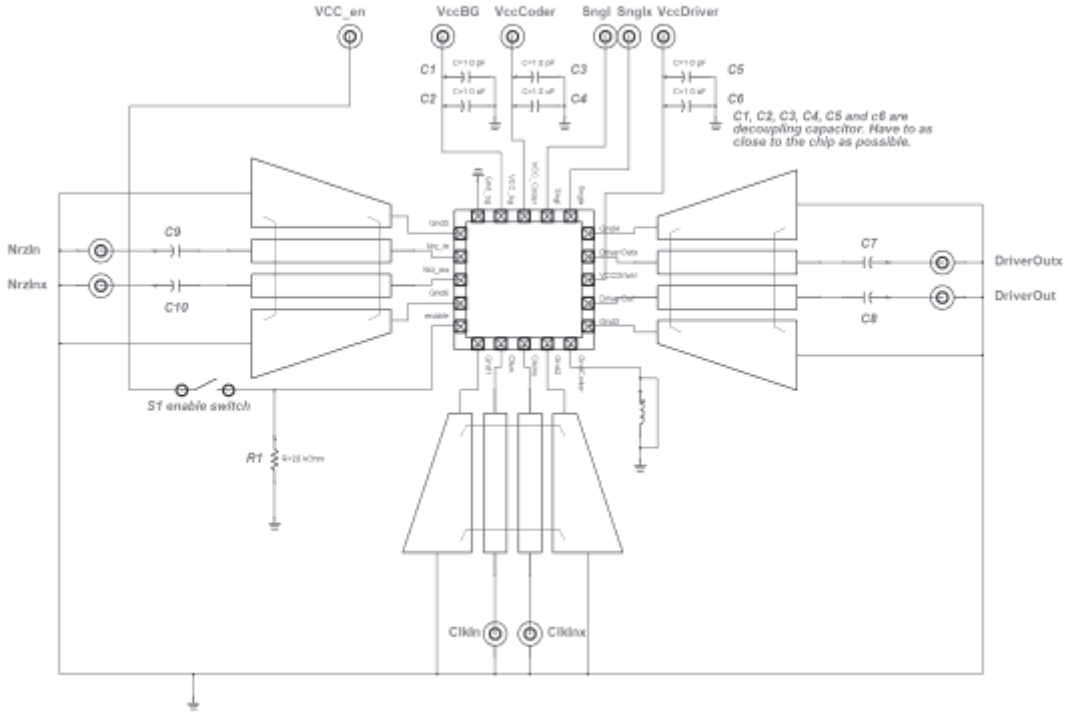
*Human Body Model

Handling

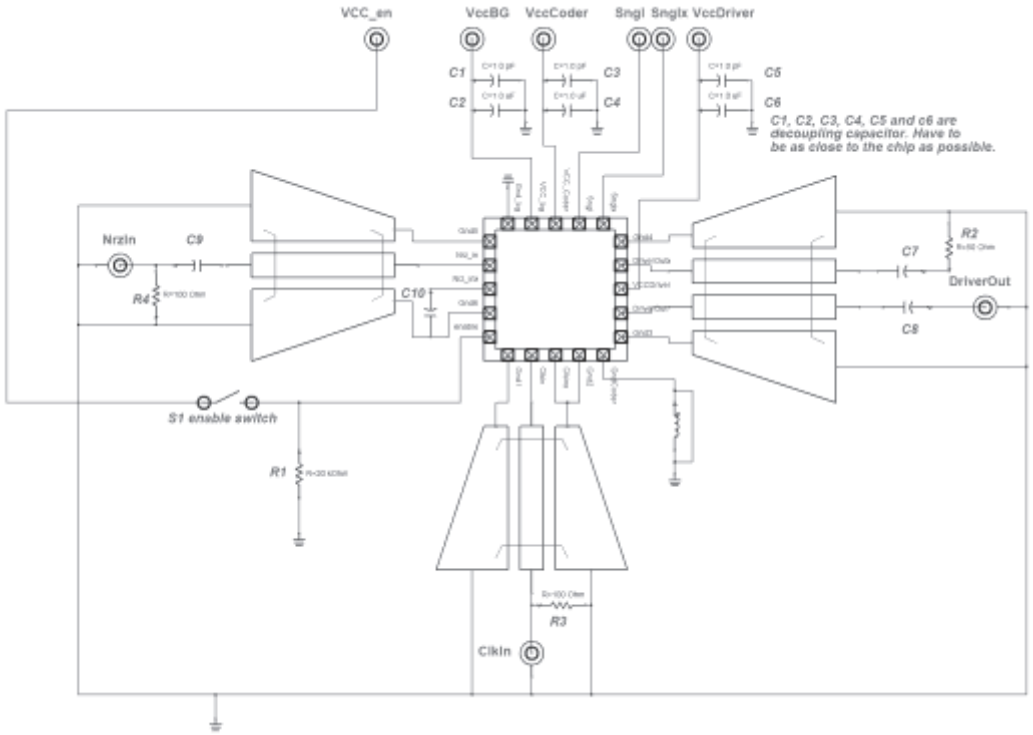
These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.

Application schematic

Differential IN and OUT



Single-ended IN and OUT



Output characteristics – simulated

Typical coder response: for -40 (1), 27 (2) and 100 (3)°C - RC

Signal:

Data rate = 20 Gb/s

NRZ

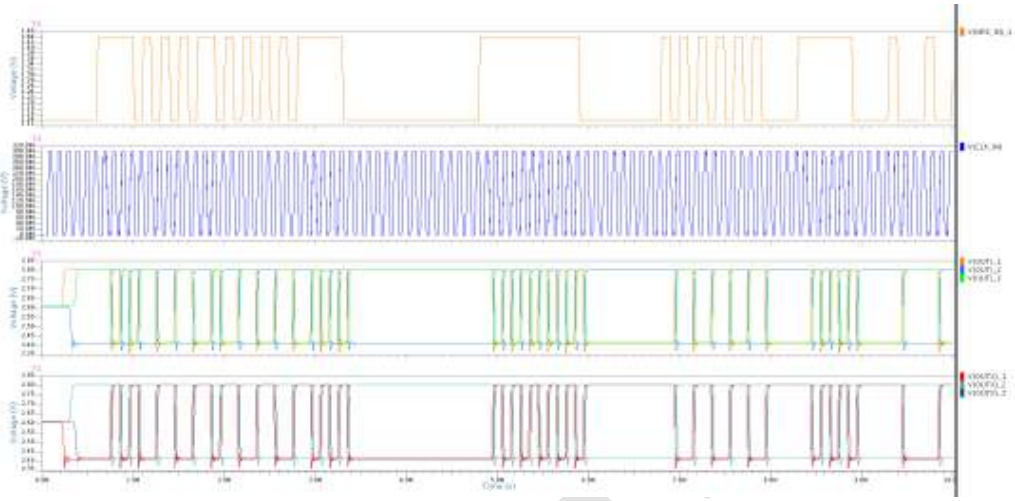
Clock:

Frequency = 20 GHz

Amplitude = 300

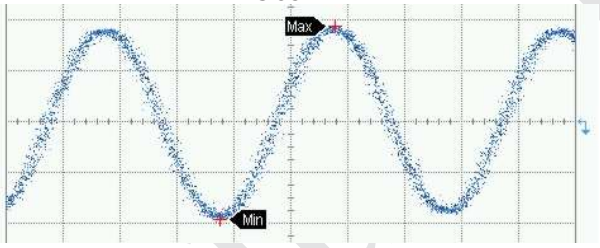
DriverOut: 50Ω loaded

DriverOutx: 50Ω loaded

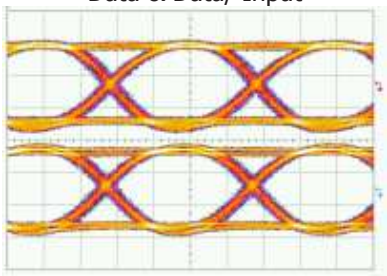


Measurement @12.5Gbps on a VWA 00070 AB (6K Housing)

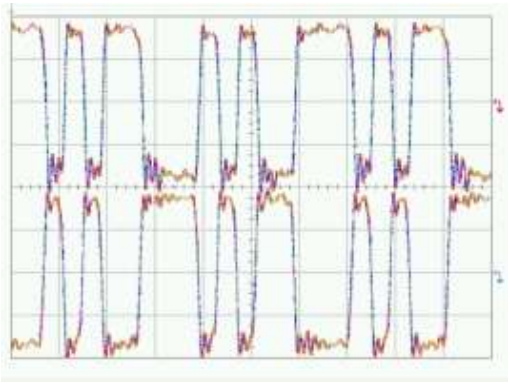
Clock In



Data & Data/ Input



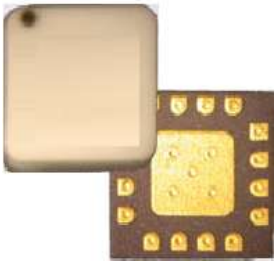
DATA Out & Out/ for an input sequence '01001111' (100mV/div; 200ps/div)

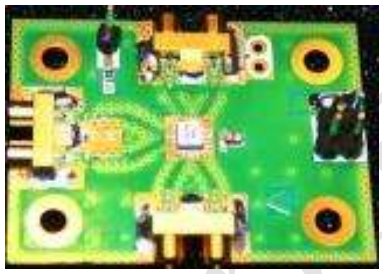


Ordering information :

Product number	Package type	Function	Min Qty order
VWA 50023 AA	Die	Differential Coder	10
VWA 00074 AB	QFN 3X3	Differential Coder	5
VWA 00078 AB	GPPO QFN Evaluation board	Differential Coder	1
VWA 00070 AB	6 K connector package	Differential Coder	1

VWA Packaged Form Proposition

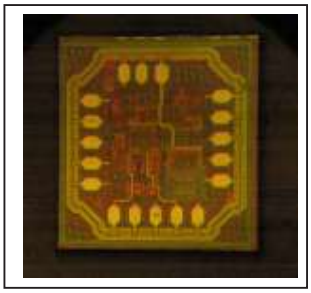




Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.

VWA 500024AAA DS Rev 0.2



NRZ to RZ
VWA-28-NRZtoRZ-SD

10 – 28 Gb/s

Description

The **VWA 50024 AA** chip is a NRZ to RZ coder for high data rate application, typically 10 to 28 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (RZ_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is synchronized by the input clock and electrically coded to the RZ format. The NRZ input signal is converted to a Return to Zero signal, each time that the clock is present at the input

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Single MZ modulator NRZ to RZ coding
- Fiber transmission

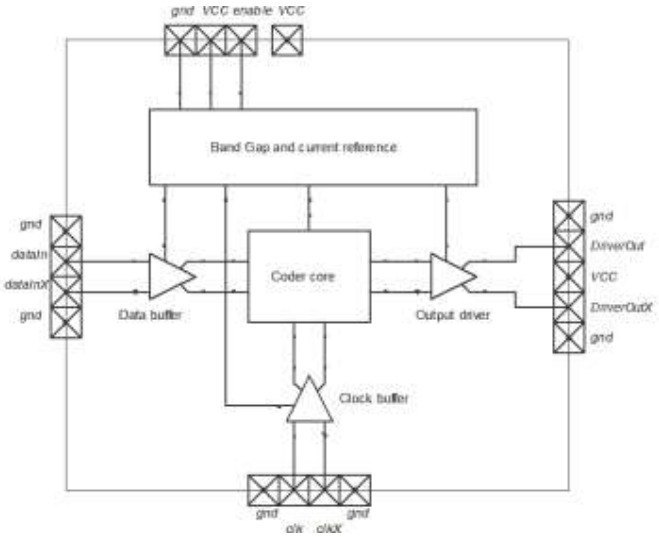
Ordering information

Part Number: VWA 50024 AA

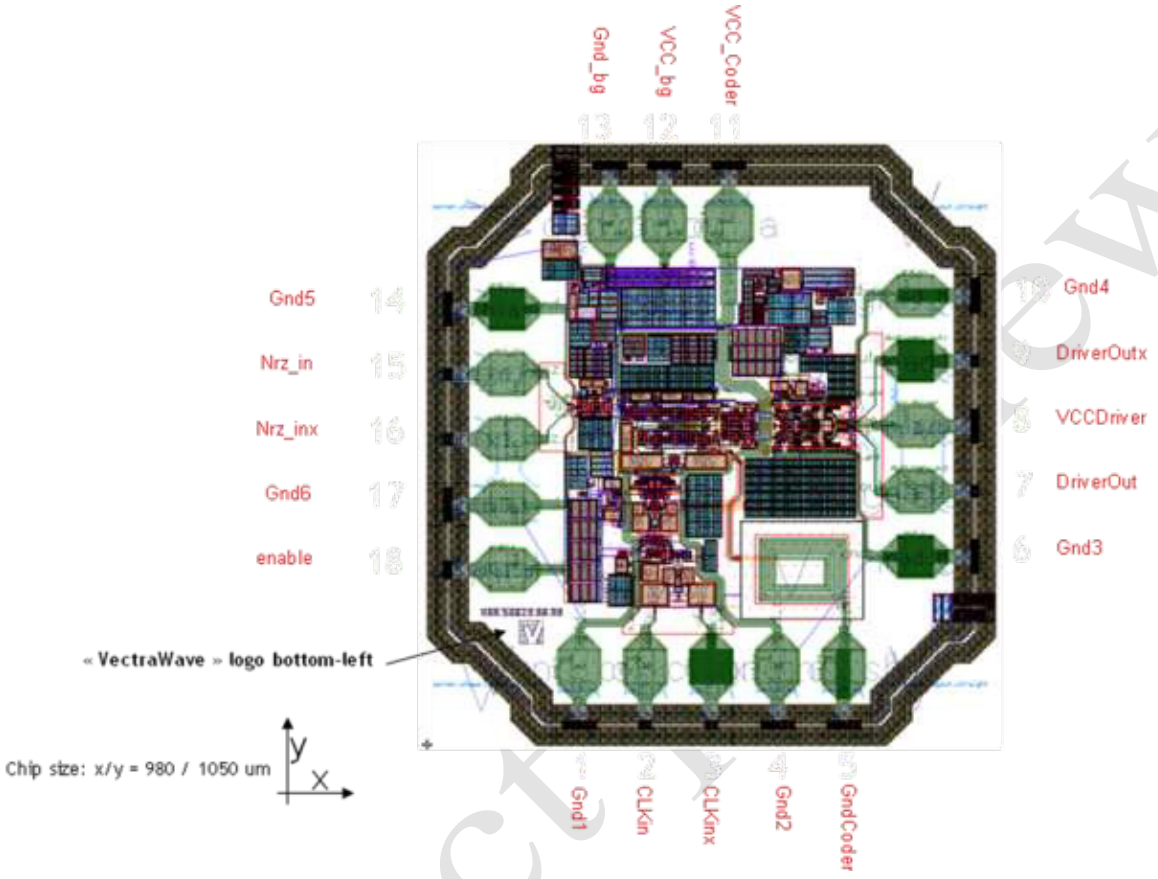
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 28Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.

VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Chip bias						
Supply voltage	**VccCoder – VccBG**	**Vcc**		3		**V**
	VccDriver		2.5	3	4	**V**
Current consumption OFF mode*	**VccCoder; enable=0; T=27°C**	**VccCoder0**		3		**nA**
	VccBG; enable=0; T=27°C	**VccBG0**	(100°C) 0.01	15	(-40°C) 28	**uA**
	VccDriver; enable=0; T=27°C	**VccDriver0**		27		**pA**

Current consumption ON mode*	**VccCoder; enable=1**	**VccCoder1**		20		**mA**
	VccBG; enable=1	**VccBG1**	(-40°C) 2		(100°C) 2.5	**mA**
	VccDriver; enable=1	**VccDriver1**		160		**mA**
Data input (Nrz_in and Nrz_inx)						
Input impedance	**Single and differential modes**	**Zin**		100		**Ω**
Amplitude range**	**Single or differential input**		2	300		**mVpp**
Clock input (Clkin and Clkinx)						
Input impedance	**Single and differential modes**			100		**Ω**
Amplitude range**	**Single or differential input**		1	300		**mVpp**
Frequency range***					25	**GHz**
Phase margin				Tbit/4		
Driver Output						
Output impedance	**Single / Differential**			50 / 100		**Ω**
Common mode voltage	**Referred to VCCDriver**			VCCDriver-0.350		**V**
Amplitude	**Single**			400		**mVpp**

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG - VccDriver**	**Vcc**	-0.5		4.6	**V**

Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

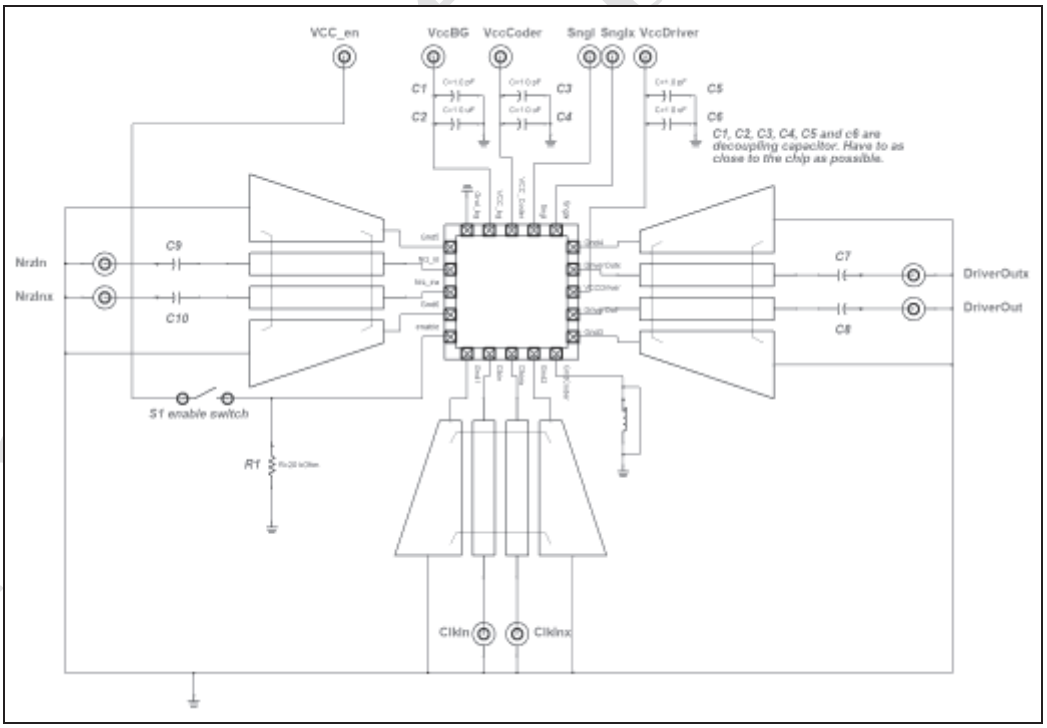
ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

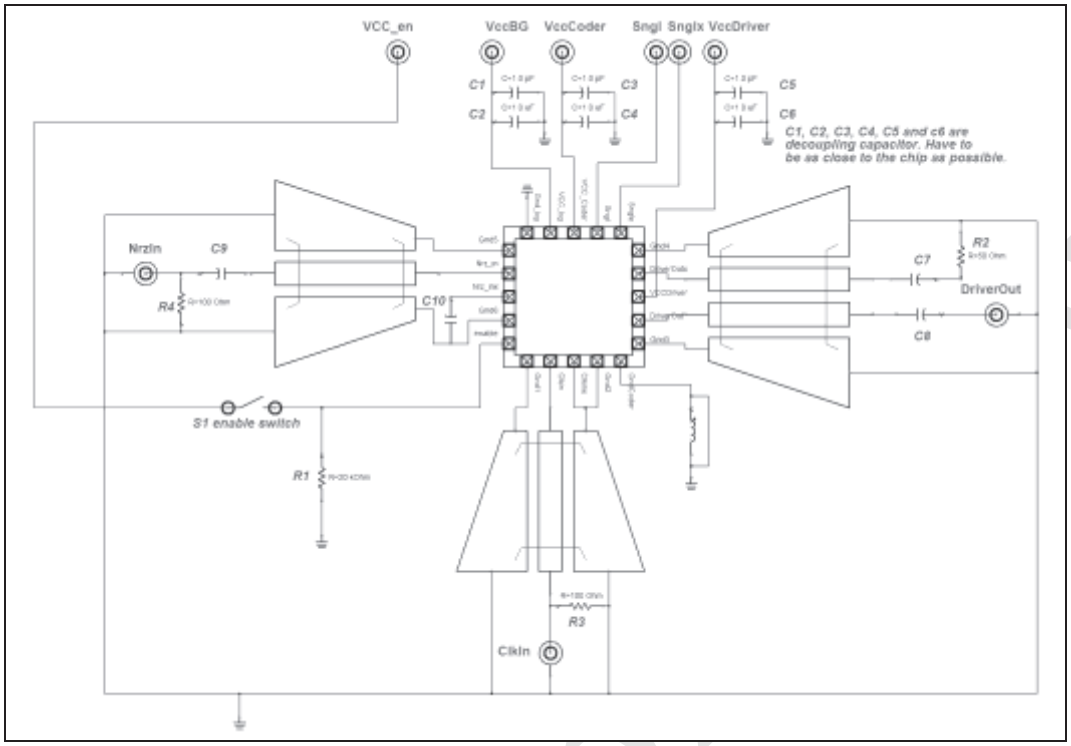
*Human Body Model

Application schematic

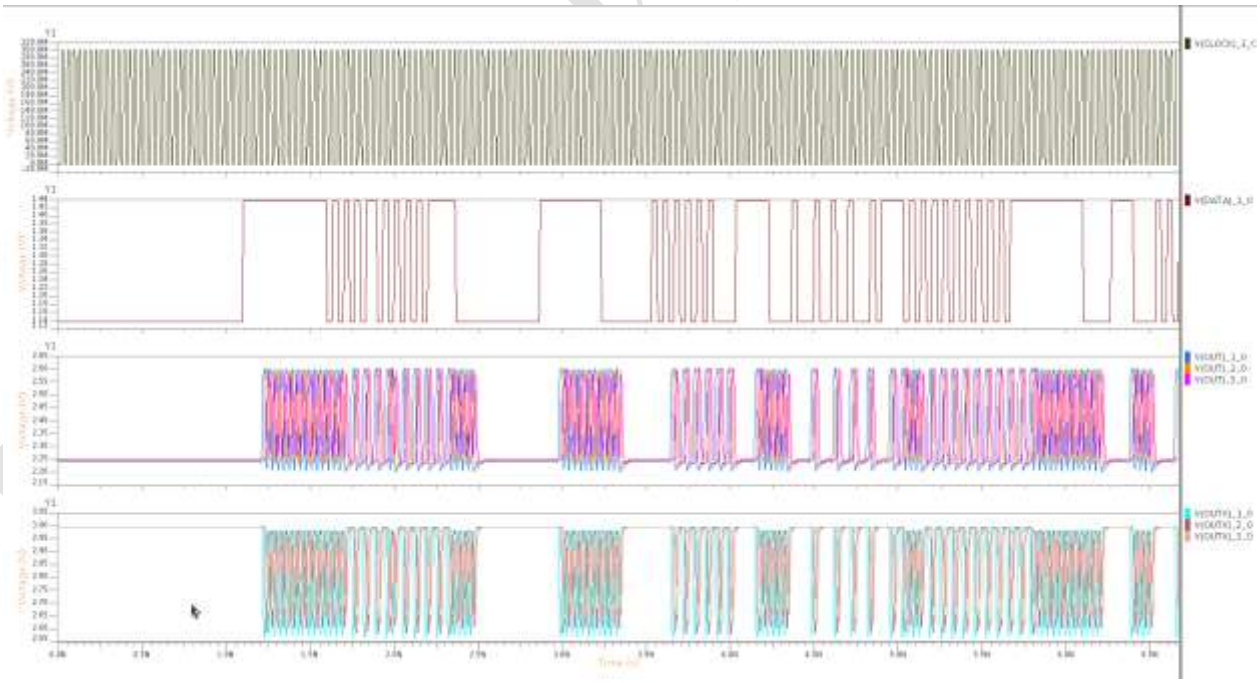
Differential IN and OUT



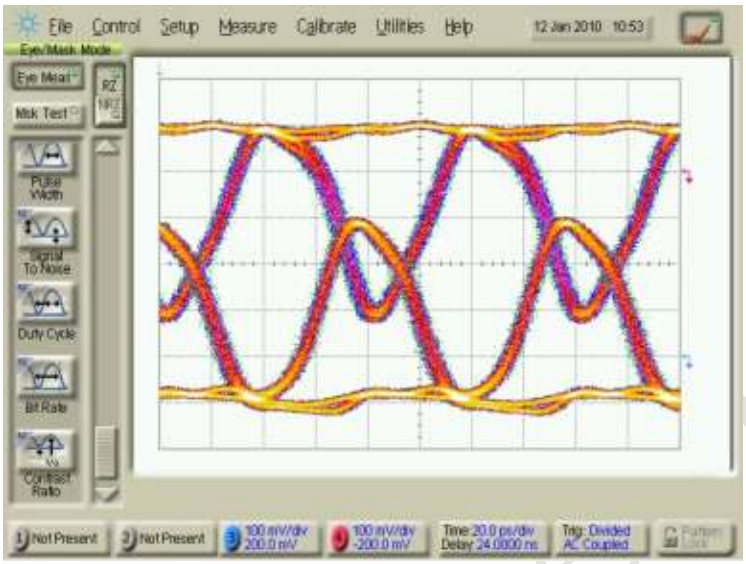
Single-ended IN and OUT



Output characteristics – simulated @30Gbps from -40 to +100°C



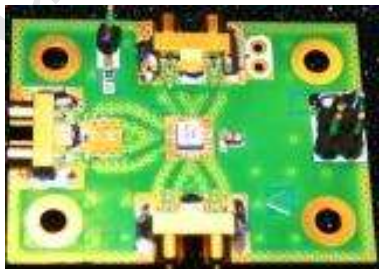
Measurement @12,5Gbps on a VWA 00071 AB (6K Housing)



Ordering information :

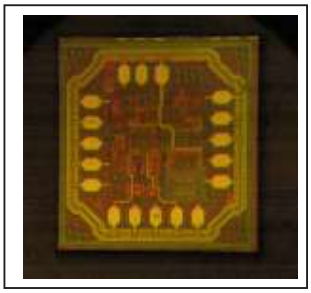
Product number	Package type	Function	Min Qty order
VWA 50024 AA	Die	NRZ to RZ_DPSK	10
VWA 00059 AA	QFN 3X3	NRZ to RZ_DPSK	5
VWA 00095 AA	GPPO QFN Evaluation board	NRZ to RZ_DPSK	1
VWA 00071 AB	6 K connector package	NRZ to RZ_DPSK	1

VWA Packaged Form Proposition



Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.



Duobinary coder
VWA-28-DUO-SD

10 – 28 Gb/s

Description

The **VWA 50029 AA** chip is a duobinary coder for high data rate application, typically 10 to 25 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (Duobinary_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is synchronized by the input clock and electrically coded to the duobinary format. The output is a 3 level signal: a logical NRZ "0" input always gives an analog "0V" output, as a logical "1" input gives alternatively either "+V" or "-V" depending on the previous "1" state.

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Duobinary TX
- Fiber transmission

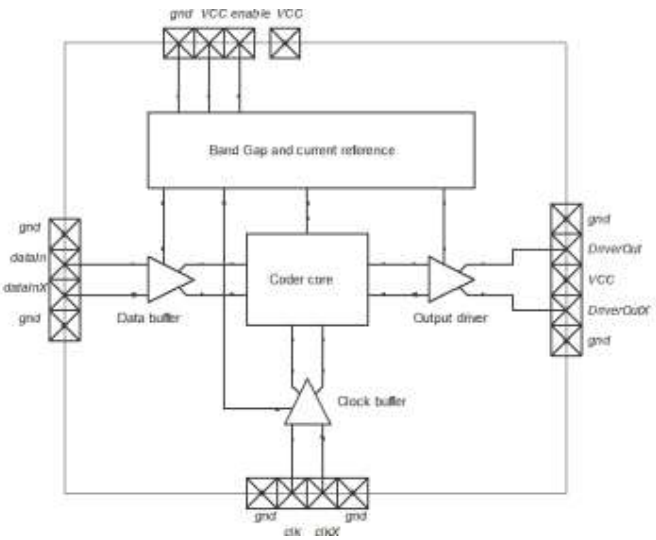
Ordering information

Part Number: VWA 50029 AA

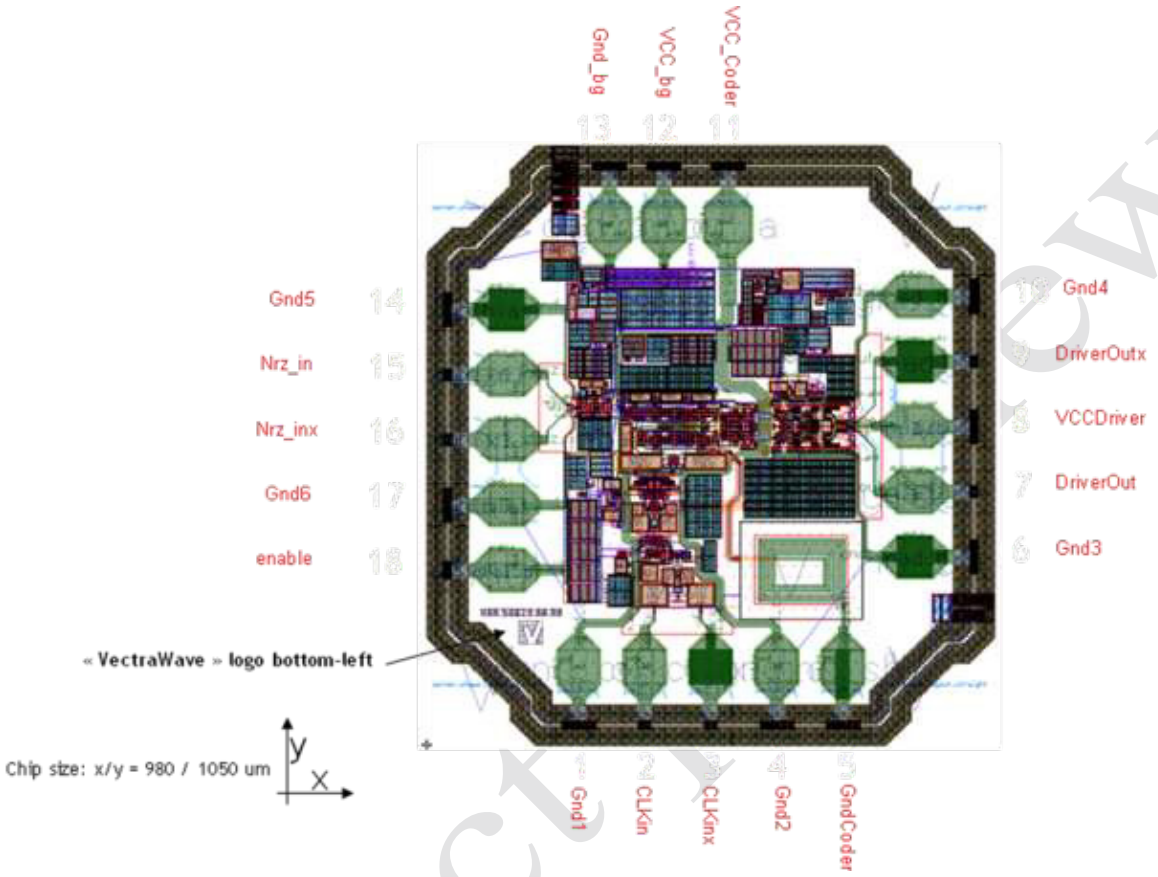
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 25Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistant with 50Ω: has to be loaded if not used.

VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistant with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
		Chip bias				
Supply voltage	VccCoder – VccBG	Vcc		3		V
	VccDriver		2.5	3	4	V
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		nA
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	uA
	VccDriver; enable=0; T=27°C	VccDriver0		27		pA
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		160		mA
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	mA
	VccDriver; enable=1	VccDriver1		20		mA
		Data input (Nrz_in and Nrz_inx)				
Input impedance	Single and differential modes	Zin		100		Ω
Amplitude range**	Single or differential input		2	300		mVpp
		Clock input (Clkin and Clkinx)				
Input impedance	Single and differential modes			100		Ω
Amplitude range**	Single or differential input		1	300		mVpp
Frequency range***					25	GHz
Phase margin				Tbit/4		
		Driver Output				
Output impedance	Single / Differential			50 / 100		Ω

Common mode voltage	**Referred to VCCDriver**			VCCDriver-0.350		**V**
Amplitude	**Single**			400		**mVpp**

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG - VccDriver**	**Vcc**	-0.5		4.6	**V**
Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

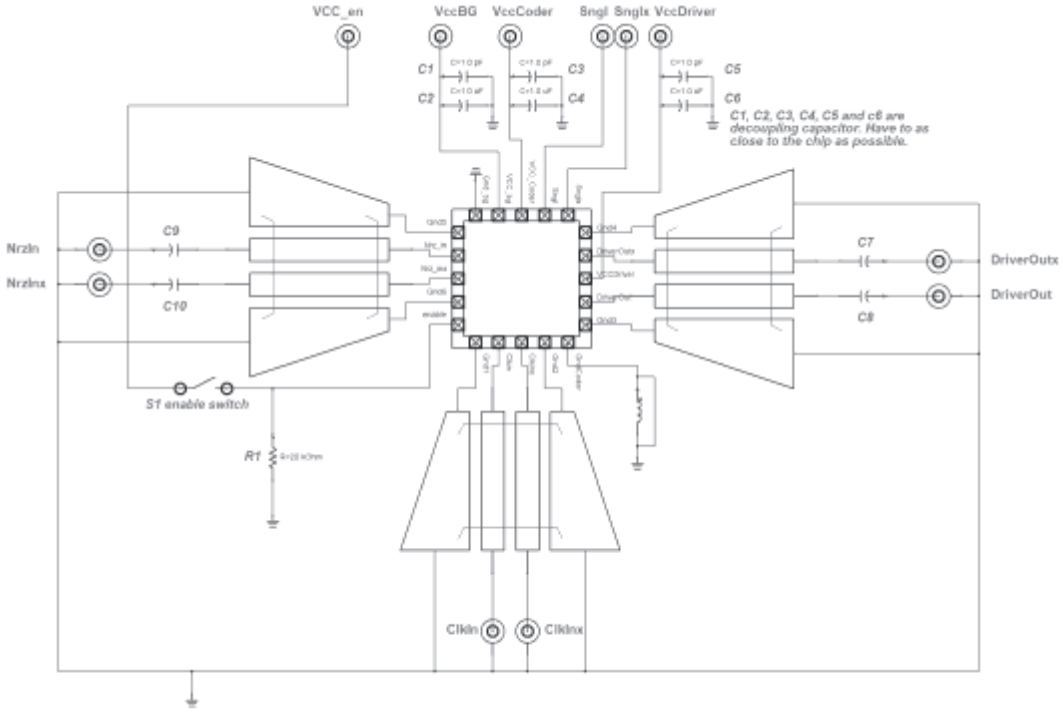
ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

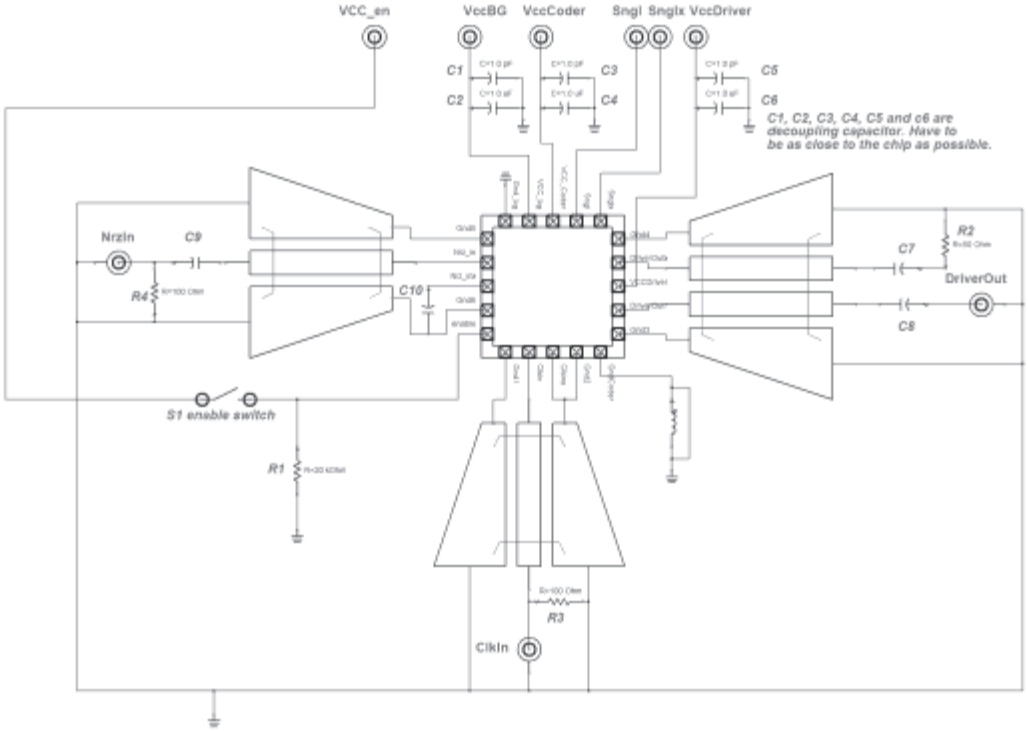
*Human Body Model

Application schematic

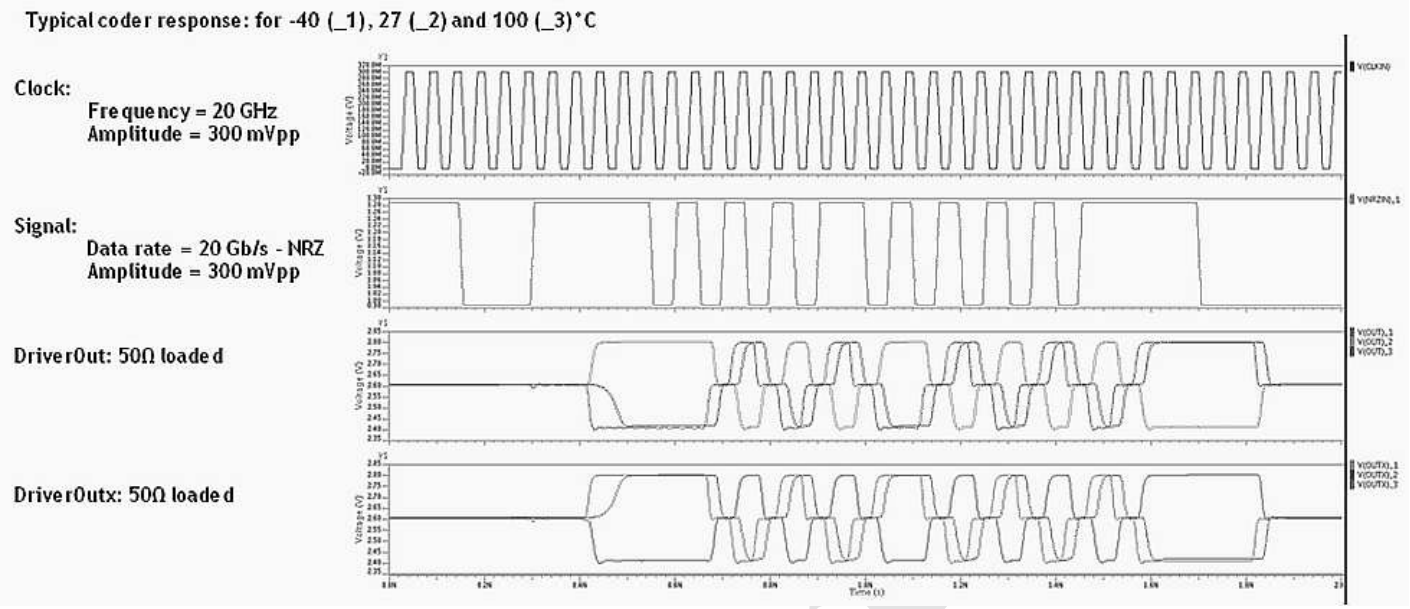
Differential IN and OUT



Single-ended IN and OUT

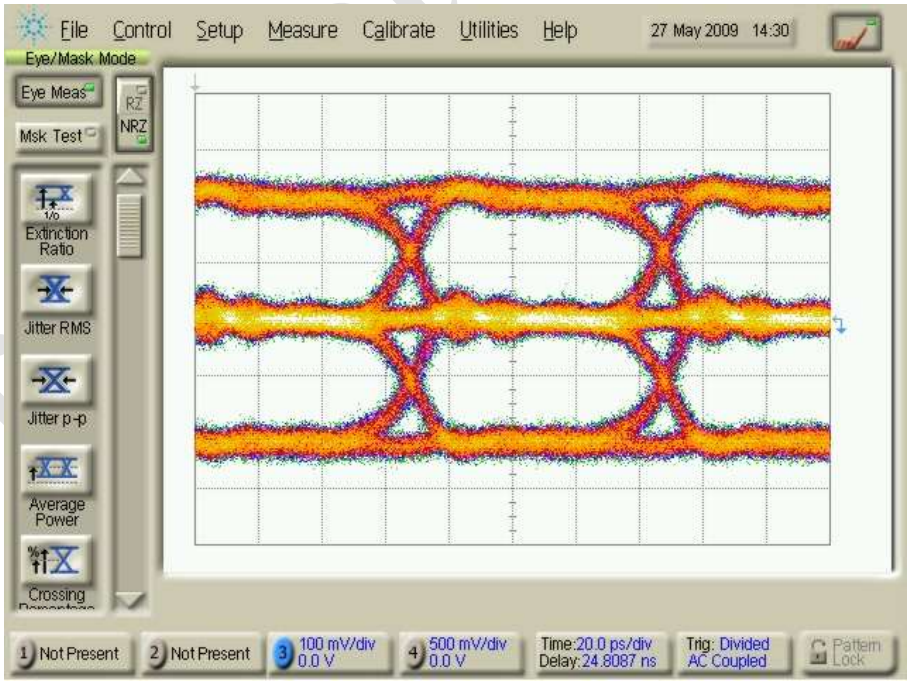


Output characteristics - simulated

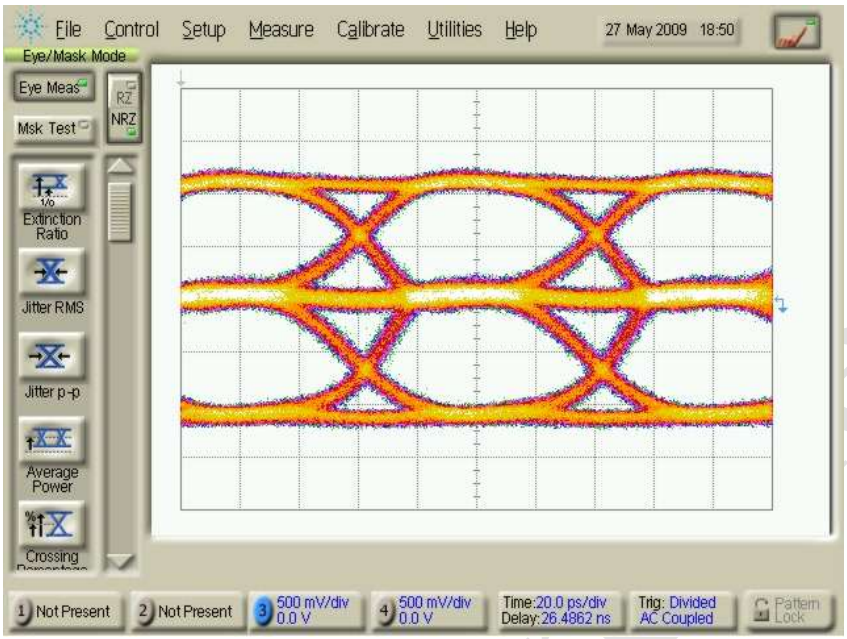


Eye diagram measurement @12.5Gbps

Measurement conditions: single-ended IN and OUT, measured directly to the chip output



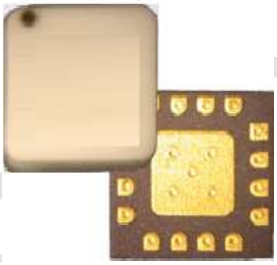
Measurement conditions: single-ended IN and OUT, measured after driver

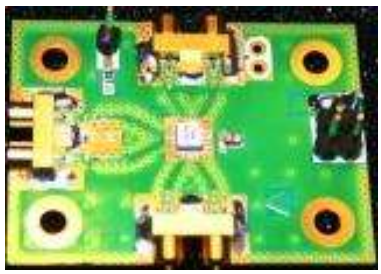


Ordering information :

Product number	Package type	Function	Min Qty order
VWA 50029 AA	Die	Duo binary coder	10
VWA 00058 AA	QFN 3X3	Duo binary coder	5
VWA 00094 AA	GPPO QFN Evaluation board	Duo binary coder	1
VWA 00072 AB	6 K connector package	Duo binary coder	1

VWA Packaged Form Proposition





Handling

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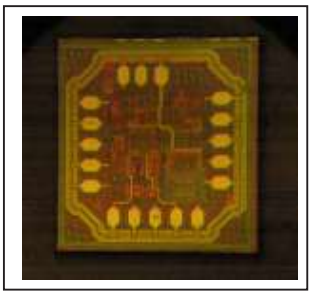
VWA 50030 AAAA DS Rev 0.3



Differential Amplifier
VWA-40-DIA-SD

DC – 40 Gb/s

Description

The **VWA 50030 AA** chip is a limiting - high gain differential amplifier for high data rate application, typically 10 to 40 Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The chip can be used in various ways:

- Single ended input to differential output transformer, by grounding through a capacitor one of the inputs.
- Limiting amplifier, using the high linear gain to saturate the input signal.
- Cross point adjustment can be done by tuning the DC levels between the two inputs.

The amplifier is a 6 stages amplifier, giving typically 60dB linear gain. When in saturation, the output amplitude is 400 mV pp single ended (800 mV differential pp).

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip (especially the output amplitude), insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the amplifier core (input buffers and amplifier core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Limiter.
- Single to differential transformation.
- Cross point control.

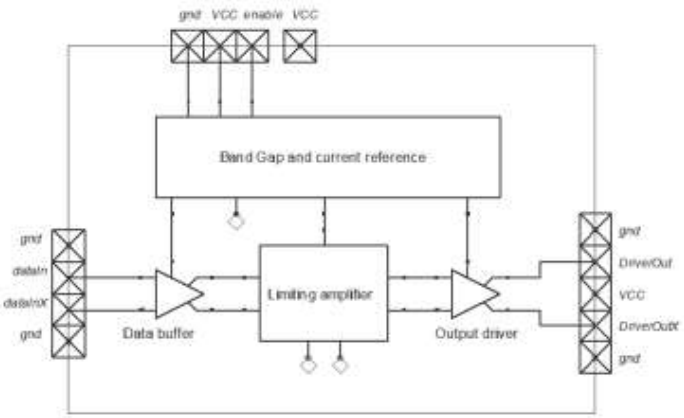
Ordering information

Part Number: VWA 50030 AA

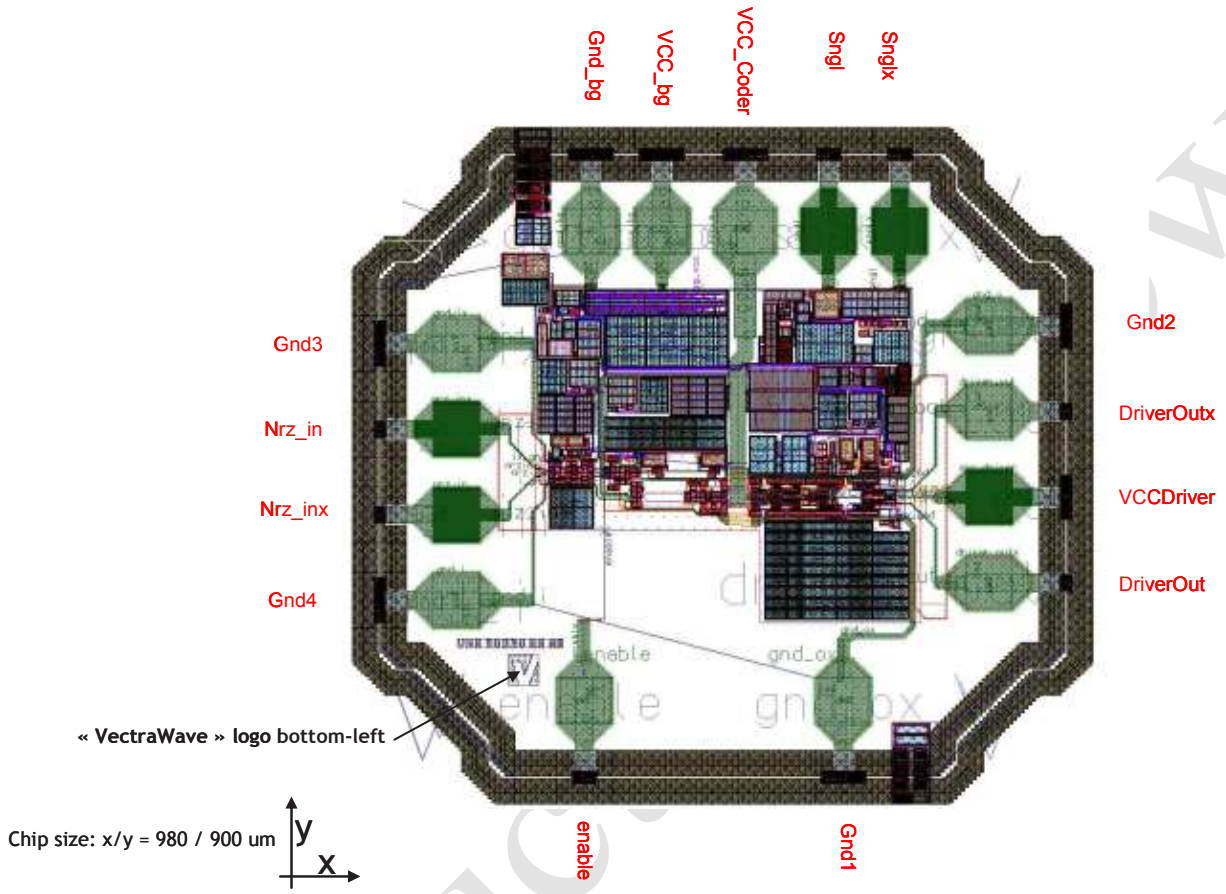
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 25Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude: 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



Name	Type	Description
enable	Digital input	Chip enable: switches the chip ON or OFF.
Gnd1*	Bias in/out	Ground for the driver output stage. To be used with Gnd2 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd2*	Bias in/out	Ground for the driver output stage. To be used with Gnd1 as ground plane for coplanar access.

Snglx	Digital out	High (VCC) if no input signal
Sngl	Digital out	High if input signal: Snglx complementary
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the amplifier core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd3*	Bias in/out	Ground for input signal access. To be used with Gnd4 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential referenced to Nrz_in.
Gnd4*	Bias in/out	Ground for input signal access. To be used with Gnd3 as ground plane for coplanar access.

- All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Chip bias						
Supply voltage	VccCoder – VccBG	Vcc		3		V
	VccDriver		2.5	3	4	V
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		nA
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	uA
	VccDriver; enable=0; T=27°C	VccDriver0		27		pA
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		90		mA
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	mA
	VccDriver; enable=1	VccDriver1		16		mA
Data input (Nrz_in and Nrz_inx)						
Input impedance	Single and differential modes	Zin		100		Ω
Amplitude range**	Single or differential input		2	300		mVpp
Frequency range***			0		40	GHz
Driver Output						
Output impedance	Single / Differential			50 / 100		Ω
Common mode voltage	Referred to VCCDriver			VCCDriver-0.350		V
Amplitude	Single			400		mVpp

* OFF → enable =“0”, ON → enable=“1”
** The Min value corresponds to the value which saturates the Driver output.
*** The frequency range is limited for low frequency, by the external decoupling capacitors.

Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	**VccCoder – VccBG - VccDriver**	**Vcc**	-0.5		4.6	**V**
Digital input	**enable**		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

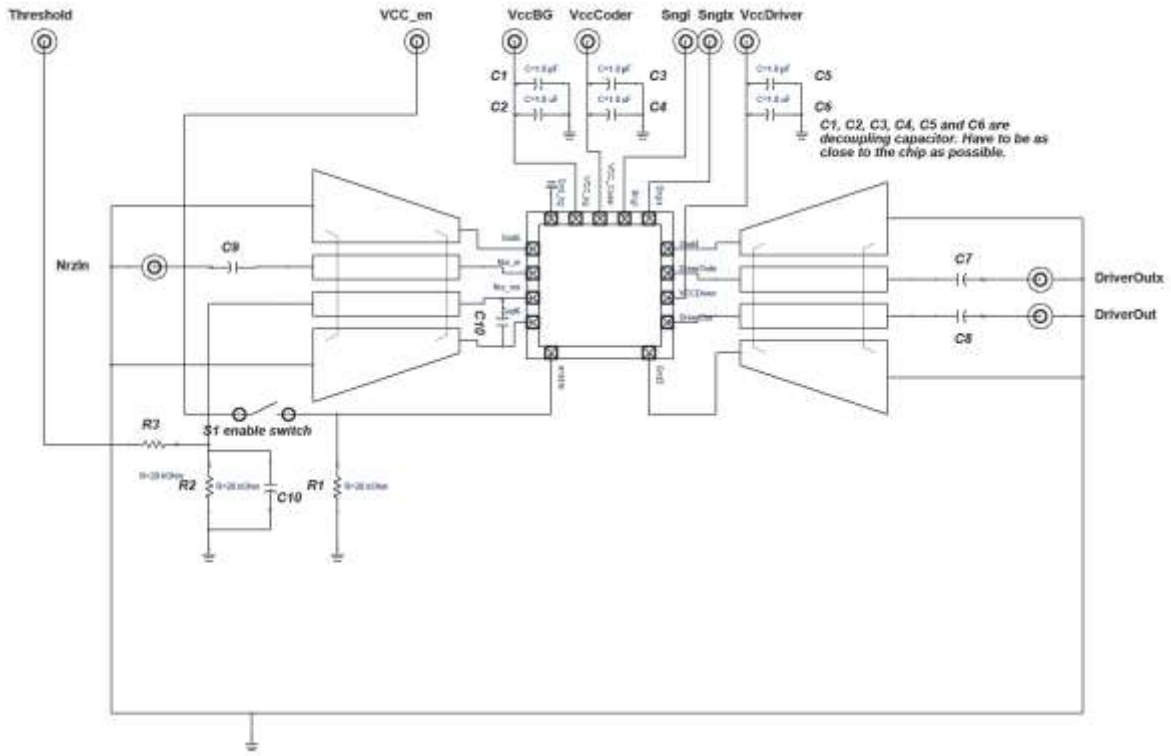
ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	**Clk, NRZin DriverOut**				0.9	**kV**
HBM* rating analog	**enable**				2.3	**kV**
HBM* rating bias	**VCC gnd**				5.7	**kV**

*Human Body Model

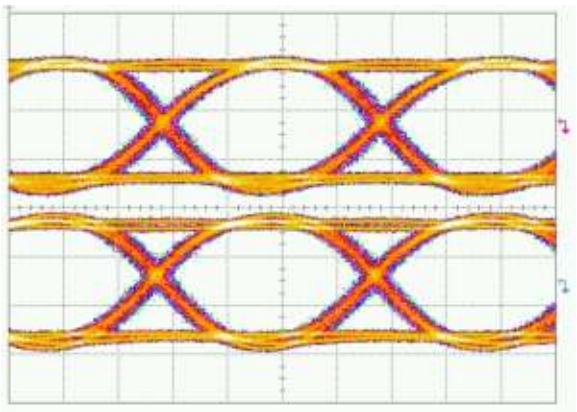
Application schematic

Single IN, Differential OUT with cross point modification

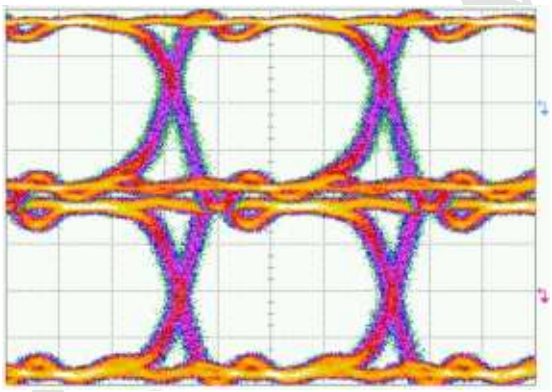


Measurement conditions on a VWA 00087 AA (6K connectors Housing):

Parameters	VEE	IEE	Data In	Data In/	T labo	Débits	Logique	trigger	Longueur trame
Conditions	-3		100	100	32	12.5	positive	12.5	2^31-1
Unités	V	mA	mV	mV	°C	Gbps		GHz	bits



Data out and Data Out/
Amplitude : 40mV/div ; Time : 20ps/div

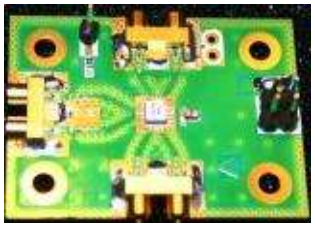


Data out and Data Out/
Amplitude : 100mV/div ; Time : 20ps/div.

Ordering information :

Product number	Package type	Function	Min Qty order
VWA 50030 AA	Die	Differential Limiting Amplifier	10
VWA 00057 AA	QFN 3X3	Differential Limiting Amplifier	5
VWA 00096 AB	GPPO QFN Evaluation board	Differential Limiting Amplifier	1
VWA 00087 AB	6 K connector package	Differential Limiting Amplifier	1

VWA Packaged Form Proposition



Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.

VWA-0R518-MP-1421

14dB Gain 0,5 to 18GHz Ultra Wideband Medium Power Amplifier Module

Description

The **VWA-0R518-MP-1421** is a broadband single stage GaAs MMIC amplifier module, which provides up to 14 dB gain from 0.5 GHz to 18 GHz and delivers +21 dBm of output power, with less than 6 dB Noise Figure within the bandwidth. This unit can be provided with a matching in phase of +/- 10°. This unit is designed for Ultra Wideband applications and is ideal for ECM, T&M, driving E/O modulator with RF signal as well as others RF applications. This amplifier has single-ended input and output, and SMA field replaceable RF connectors (male or female).

Features

- Ultra Wideband
- High Gain
- Low Noise Figure
- High power
- 50 Ohm impedance
- Single +12V supply

Typical Characteristics (25°C)

Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	18			GHz
Low Frequency Response (-3 dB)	BW_{Low}			500	MHz
Averaged Gain	G	14		17	dB
Gain Flatness	ΔG	-1,5		+1,5	dB
Noise Figure (@ +55°C)	NF			6	dB
Input Return Loss	S11		-8	-10	dB
Output Return Loss	S22		-8	-10	dB
Output Power @ 1dB gain compression	P_{1dB}	+21			dBm
Bias Voltage	V_{bias}	+10	+12	+ 15	V
Drive Current	I_d		260		mA

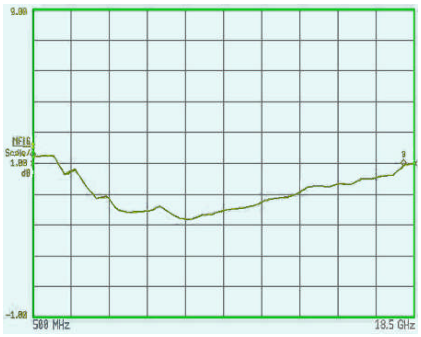
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-20		+70	°C
Storage temperature	T_{stg}	-55		+85	°C

Absolute maximum ratings

Maximum ratings	Symbols	Min	Typ	Max	Units
Supply Voltage	$V_{bias\ max}$			+15	V
Lead soldering temperature				250	°C

Typical measurements

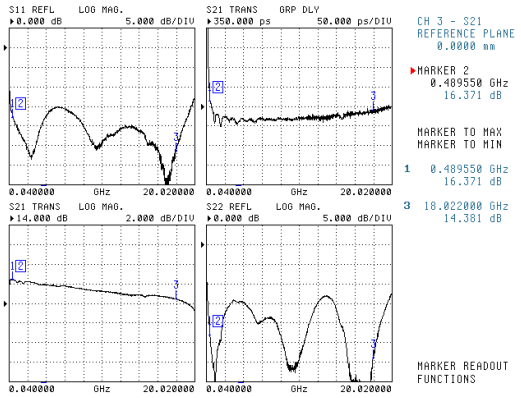
Noise Figure



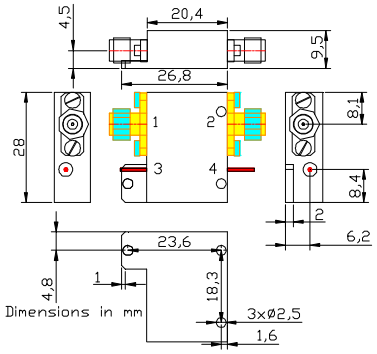
Output Power @ 1dB compression

P 1dB (dBm)	
0.5GHz	22.8
2GHz	23.0
10GHz	22.5
16GHz	22.0
18GHz	21.5

S Parameters



Mechanical characteristics (dimensions in mm)



Pin out

Pin Nb	Designation
1	Input
2	Output
3	V_{bias}
4	Ground

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-0R518-MP-1421** module.

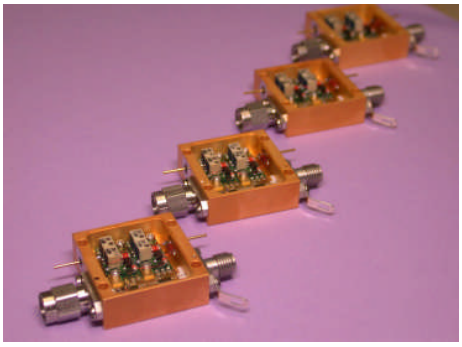
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Part number	Operating temp. °C	Connector In	Connector Out
VWA 00005 BA	-20 / + 70	SMA female	SMA female

Options on demand:

- Input and output RF connectors
- Operating temperature -40/+85°C



VWA-0R518-MP-2521

25dB Gain 0,5 to 18GHz Ultra Wideband Medium Power Amplifier Module

Description

The **VWA-0R518-MP-2521** is a broadband dual stage GaAs MMIC amplifier module, which provides up to 25 dB gain from 0.5 GHz to 18 GHz and delivers +21 dBm of output power, with less than 5.5 dB Noise Figure within the bandwidth. This unit is designed for Ultra Wideband applications and is ideal for ECM, T&M, driving E/O modulator with RF signal as well as others RF applications. This amplifier has single-ended input and output, and SMA field replaceable RF connectors (male or female).

Features

- Ultra Wideband
- Very High Gain
- Very Low Noise Figure
- High power
- 50 Ohm impedance
- Single +12V supply

Typical Characteristics (25°C)

Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	18			GHz
Low Frequency Response (-3 dB)	BW_{Low}			500	MHz
Averaged Gain	G	24		29	dB
Gain Flatness	ΔG	-1,5		+1,5	dB
Noise Figure (@ +55°C)	NF			5,5	dB
Input Return Loss	S11		-8	-10	dB
Output Return Loss	S22		-8	-10	dB
Output Power @ 1dB gain compression	P_{1dB}	+21			dBm
Bias Voltage	V_{bias}	+10	+12	+ 15	V
Drive Current	I_d		400		mA

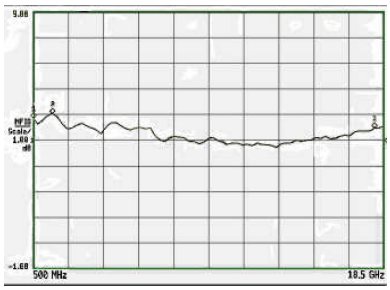
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-20		+70	°C
Storage temperature	T_{stg}	-55		+85	°C

Absolute maximum ratings

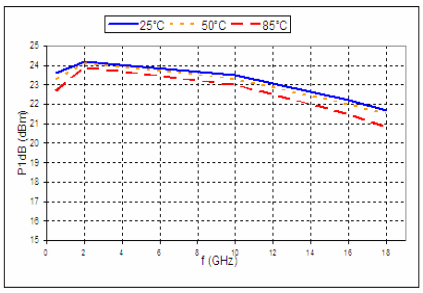
Maximum ratings	Symbols	Min	Typ	Max	Units
Supply Voltage	$V_{bias\,max}$			+15	V
Lead soldering temperature				250	°C

Typical measurements

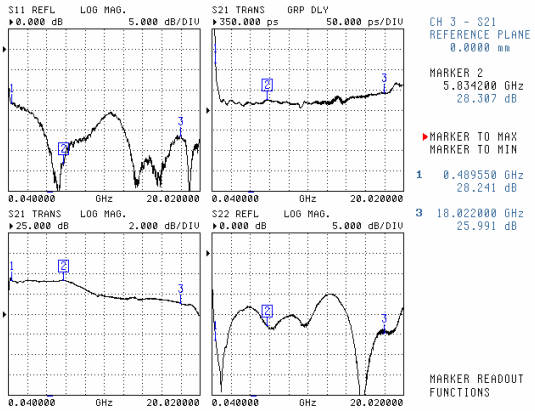
Noise Figure



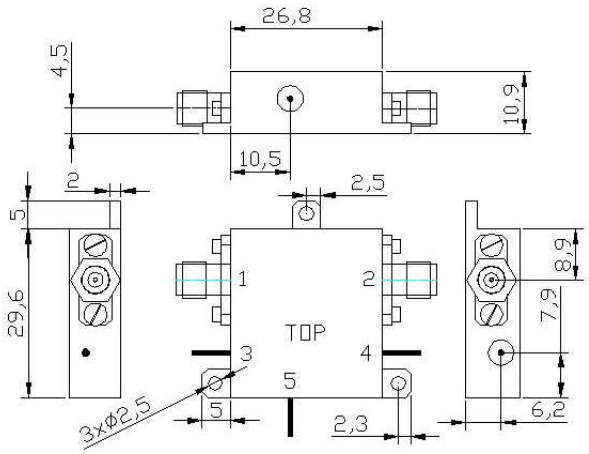
Output Power @ 1dB compression



S Parameters



Mechanical characteristics (dimensions in mm)



Pin out

Pin Nb	Designation
1	Input
2	Output
3	Vbias
4	Ground
5	V_c

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-0R518-MP-2521 module**.

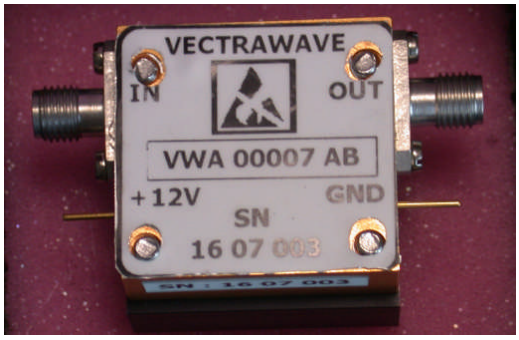
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Part number	Operating temp. °C	Connector In	Connector Out
VWA 00027 AA	-20 / + 70	SMA female	SMA female

Options on demand:

- Input and output RF connectors
- Operating temperature -40/+85°C



VWA-00R12-MP-2320

23dB Gain 10MHz to 2GHz High IP3
Medium Power Amplifier Module

Description

The **VWA-00R12-MP-2320** is a broadband dual stage GaAs MMIC amplifier module, providing up to 23 dB gain from 10 MHz to 2 GHz and delivering up to +24 dBm output power, with less than 7.5 dB Noise Figure within the Bandwidth. This unit is designed for Ultra Wideband applications and is ideal for ECM, T&M, driving E/O modulator with RF signal as well as others RF applications. This amplifier has single-ended input and output, and SMA field replaceable RF connectors (male or female).

Features

- High Linearity
- High power
- High Gain
- Wideband
- Low Noise Figure
- 50 Ohm impedance
- Single +12V supply

Typical Characteristics (25°C)

Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	2			GHz
Low Frequency Response (-3 dB)	BW_{Low}			10	MHz
Averaged Gain	G		23		dB
Gain Flatness	ΔG	-1		+1	dB
Noise Figure (@ +55°C)	NF			8,5	dB
Input Return Loss	S11		-8	-10	dB
Output Return Loss	S22		-8	-10	dB
Output Power @ 1dB gain compression	P_{1dB}	+20	+24		dBm
Bias Voltage	V_{bias}	+10	+12	+ 15	V
Drive Current	I_d		400		mA

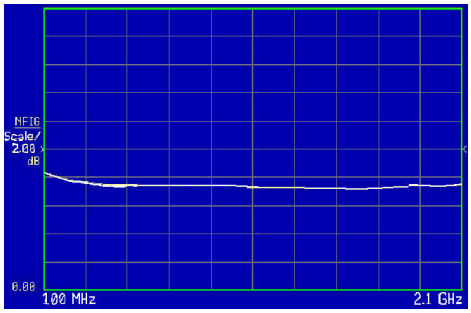
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-20		+70	°C
Storage temperature	T_{stg}	-45		+85	°C

Absolute maximum ratings

Maximum ratings	Symbols	Min	Typ	Max	Units
Supply Voltage	$V_{bias\ max}$		+12	+15	V
Lead soldering temperature				250	°C

Typical measurements

Noise Figure

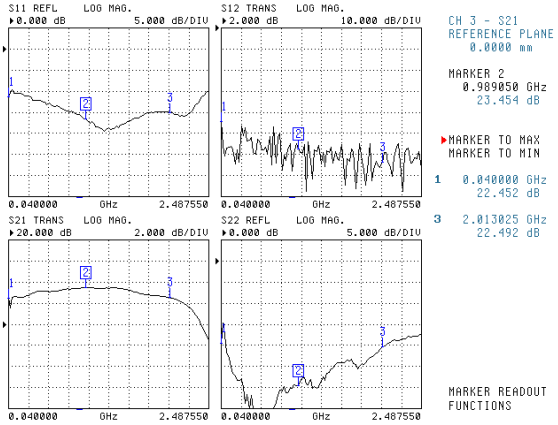


Output Power @ 1dB compression

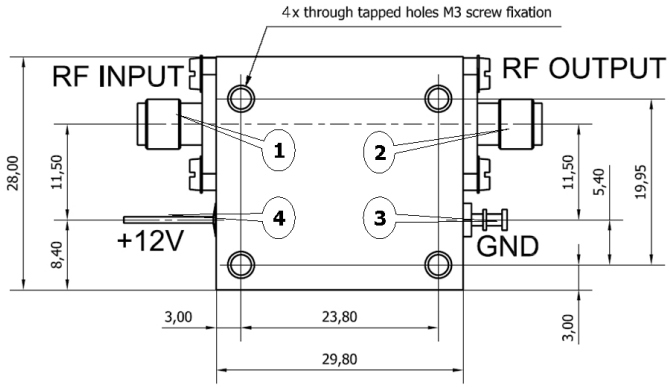
P 1dB (dBm)	
10MHz	24.7
100MHz	24.7
500MHz	25
2GHz	24.3

IP3	+33dBm
Harmonic @ output ≤+20dBm	-27dBc
Spurious	<-60dBc

S Parameters



Mechanical characteristics (dimensions in mm)



Pin out

Pin Nb	Designation
1	Input
2	Output
3	Ground
4	V_{bias}

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-00R12-MP-2320** module.

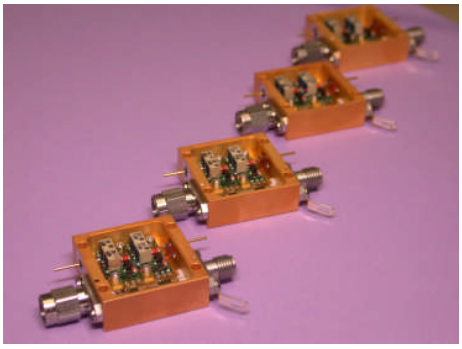
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Part number	Operating temp. °C	Connector In	Connector Out
VWA 00007 AA	-20 / + 70	SMA female	SMA female

Options on demand:

- Input and output RF connectors
- Operating temperature -40/+85**°C**



VWA-0R518-MP-2521

25dB Gain 0,5 to 18GHz Ultra Wideband Medium Power Amplifier Module

Description

The **VWA-0R518-MP-2521** is a broadband dual stage GaAs MMIC amplifier module, which provides up to 25 dB gain from 0.5 GHz to 18 GHz and delivers +21 dBm of output power, with less than 5.5 dB Noise Figure within the bandwidth. This unit is designed for Ultra Wideband applications and is ideal for ECM, T&M, driving E/O modulator with RF signal as well as others RF applications. This amplifier has single-ended input and output, and SMA field replaceable RF connectors (male or female).

Features

- Ultra Wideband
- Very High Gain
- Very Low Noise Figure
- High power
- 50 Ohm impedance
- Single +12V supply

Typical Characteristics (25°C)

Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	18			GHz
Low Frequency Response (-3 dB)	BW_{Low}			500	MHz
Averaged Gain	G	24		29	dB
Gain Flatness	ΔG	-1,5		+1,5	dB
Noise Figure (@ +55°C)	NF			5,5	dB
Input Return Loss	S11		-8	-10	dB
Output Return Loss	S22		-8	-10	dB
Output Power @ 1dB gain compression	P_{1dB}	+21			dBm
Bias Voltage	V_{bias}	+10	+12	+ 15	V
Drive Current	I_d		400		mA

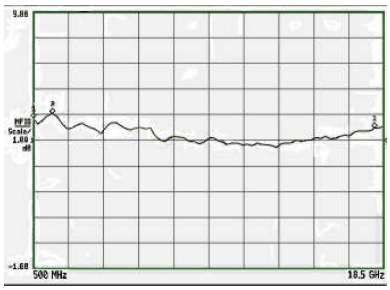
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-20		+70	°C
Storage temperature	T_{stg}	-55		+85	°C

Absolute maximum ratings

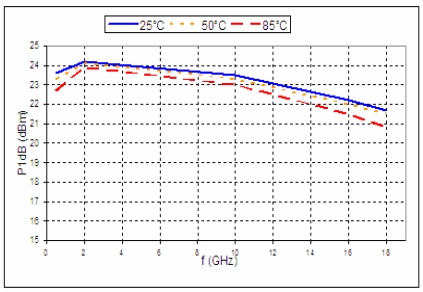
Maximum ratings	Symbols	Min	Typ	Max	Units
Supply Voltage	$V_{bias\ max}$			+15	V
Lead soldering temperature				250	°C

Typical measurements

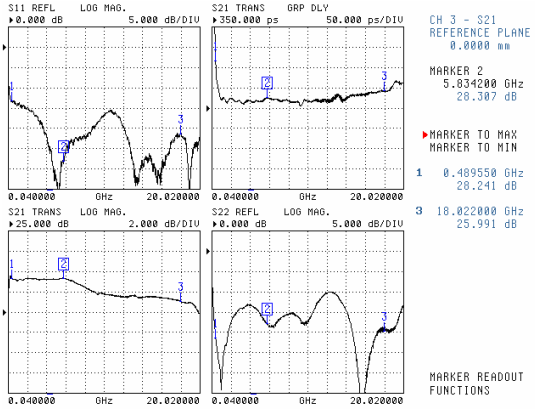
Noise Figure



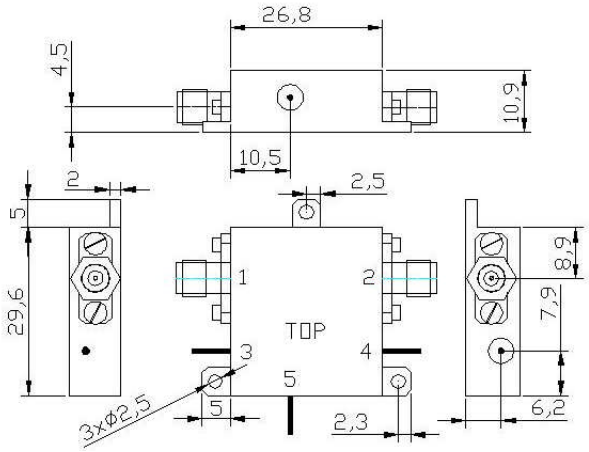
Output Power @ 1dB compression



S Parameters



Mechanical characteristics (dimensions in mm)



Pin out

Pin Nb	Designation
1	Input
2	Output
3	Vbias
4	Ground
5	V_c

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-0R518-MP-2521 module**.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Part number	Operating temp. °C	Connector In	Connector Out
VWA 00027 AA	-20 / + 70	SMA female	SMA female

Options on demand:

- Input and output RF connectors
- Operating temperature -40/+85°C

VWA-000267 ABAA

8,5 to 11,5 GHz – 27 dB – +39dBm
High Power Amplifier MMIC

Description

The **VWA-000267-ABAA** is a 3 Stages analog High power Surface Mount Package amplifier operating in the frequency range 8 to 12 GHz.

The SMD package include is a cascaded 3 stages amplifier designed in 0.25µm pHEMT process, and its decoupling circuit interfaces.

The devices is capable of more than +39 dBm output power at P sat, and provide 27dB of large signal gain from 9 to 11 GHz with less than 0,5 dB of Gain variation. The package has been optimized to provide high efficiency, supply current is as low as 2,2 A with VD=+8V, when delivering +39 dBm output power, in pulse mode.

GDSII file is available for mechanical design.

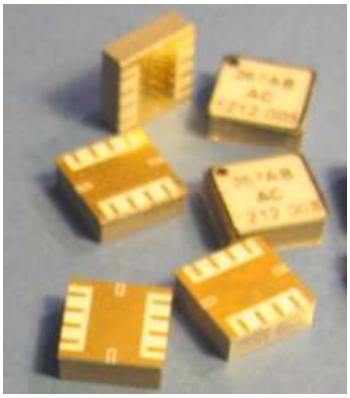
Features

- 3 stages High Power pHEMT GaAs Amplifier
- Small Surface Mount Package Device
- Wide band : 8,5 to 11,5 GHz
- High Output Psat > +39 dBm
- Large signal gain : 27dB
- 50Ω, AC coupled RF input and output,
- Power supply: 2,2 A @ +8 V; Vg=-1,4 V
- 8 x 8 x 3 mm

Applications

- X band High Power amplifier
- Broadband communication
- Radar
- Test and measurement

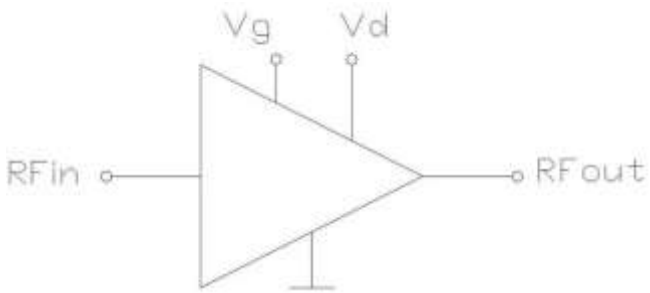
Dimensions



(8 X 8 X 3 mm)

Ordering information

Product code
VWA 000267 AB, SMD Device
VWA 000267 AB, EVB, with power supply



Functional Block Diagram

Typical Characteristics:

Tamb = 25°C, VD = +8V, ID = 2,2A, measured in pulsed mode for F= 10 KHz and duty cycle 10%.

Parameter measured in pulse mode	Symbol	Min	Typ	Max	Unit
Frequency range	F	8		12	GHz
Small signal Gain from 8 to 12 GHz	G	24			dB
Large signal Gain flatness from 9 to 11 GHz	ΔG		+/- 0,25		dB
Input adaptation from 8 to 12 GHz	S11		10		dB
Output adaptation from 8 to 12 GHz	S22		10		dB
Saturated output power	PSat		+39		dBm
Operating Drain supply voltage	VD		8		V
Supply current total for Vg= -1,4V	ID		2,2		A

Environmental parameters

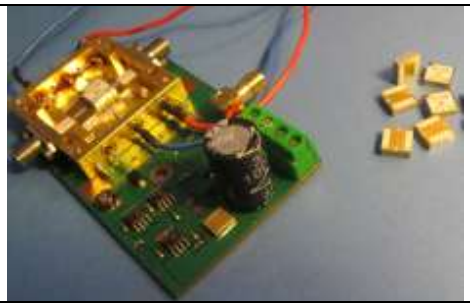
Environment Parameters	Symbols	Min	Max	Units
Storage temperature	Tst	-55	+85	°C
Operating temperature	Top	-40	+85	°C

Absolute maximum ratings

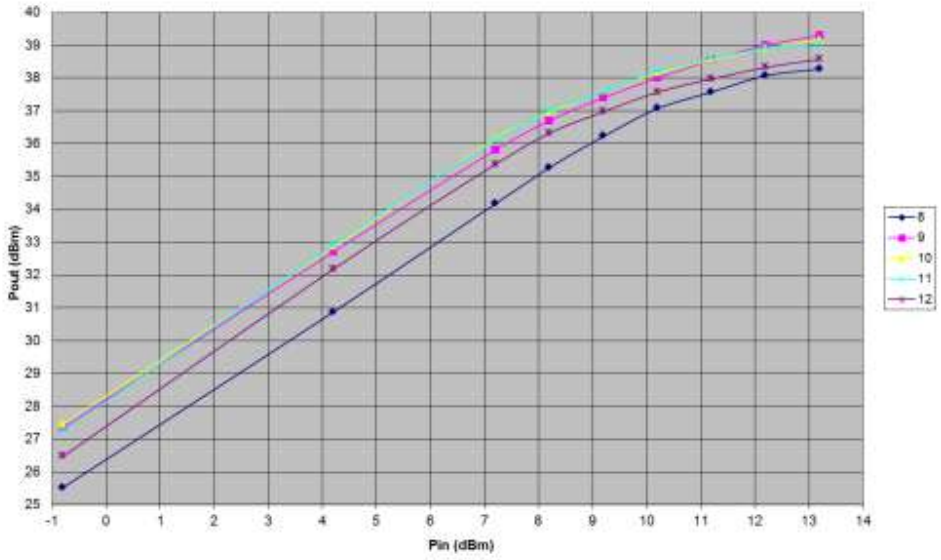
Maximum ratings	Symbols	Min	Max	Units
Compression level	Cmp		6	dbc
Drain Voltage without RF input	VD		10	V
Supply Quiescent current	ID		2,8	A
Supply current in saturation	ID_Sat		4	A
RF input power (In)	Pin max		+15	dBm

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

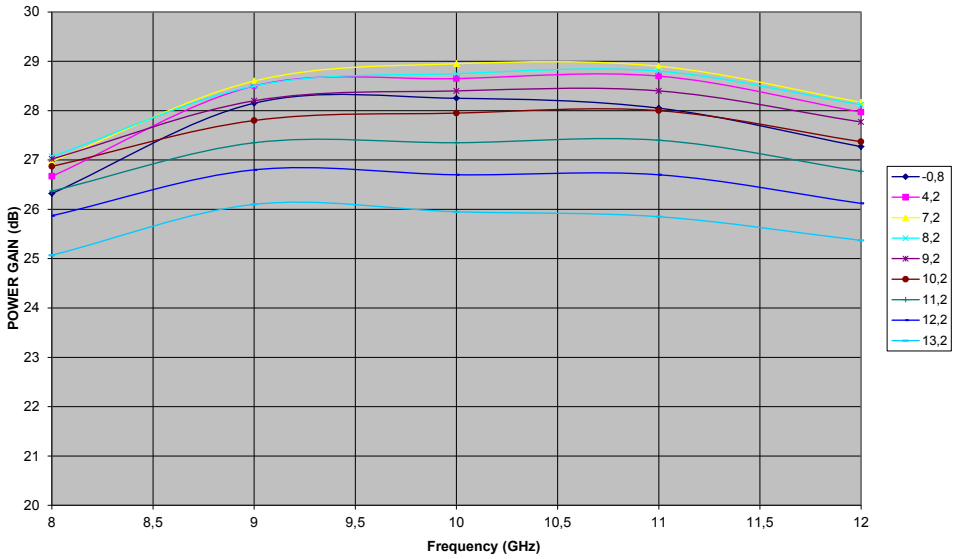
Typical test results

Test in pulse mode on evaluation board: At Room temperature. - Pulse width 10µs - Duty cycle 10% - Vd pulsed = 8V	

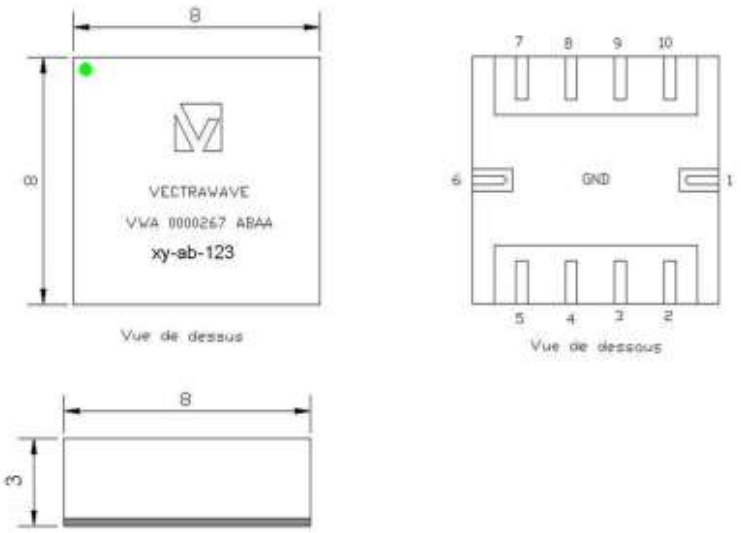
Pout = f (Pin) from 8 to 12 GHz



Gain = f (Pin) from 8 to 12 GHz



Package dimensions (mm)



Pin Out

Pin	Definition
1	RF Input
2	Vd
3	Vg
4	GND
5	Vd

Pin	Definition
6	RF Output
7	Vd
8	GND
9	Vd
10	Vg

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-0000267-ABAA** SMD device.

10G-PSD-7

X Band analog phase shifter with integrated MPA

Description

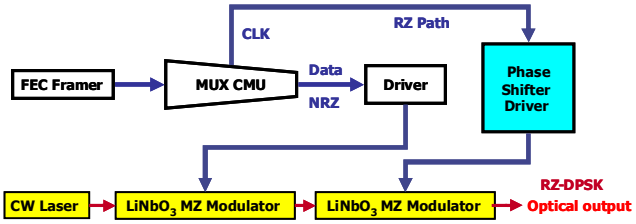
The **10G-PSD-7** is an analog phase shifter with integrated variable gain amplifier and output power amplifier in SMD package.
The device is capable of more than 360° phase shift (up to 600°), and is working from 8 to 12 GHz. The output amplifier is designed to deliver 7Vpp (up to 8Vpp) with low distortion. The variable gain amplifier has a wide dynamic range, from -10dB to +30 dB gain.
A power detector, with reference diode, is also included, giving a direct measurement of the output power.

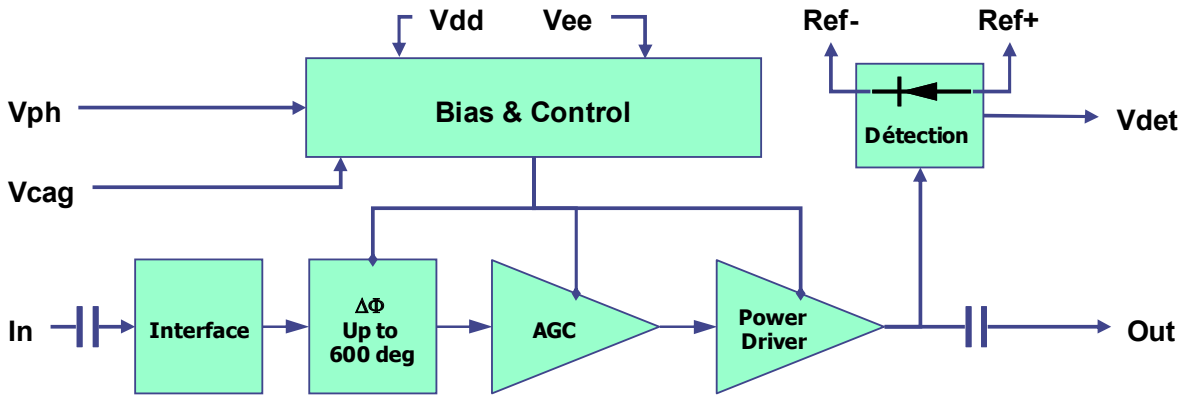
Applications

- X band phase control
- Radar
- Fiber transmission
- DPSK
- 10Gps

Features

- 16x16 mm² SMD
- 48 pins w/1mm pitch
- 50Ω RF Single ended input and output
- AC coupled
- Wide band : 8 – 12 GHz
- Wide phase shift from 0 to >360°
- Low power <4W @ 7Vpp
- +8V and -3.3V voltage supply
- High output level, up to 8Vpp
- Wide dynamic gain control -10dB to +30dB
- Phase shift command
- Gain command
- Output level detection
- Ref diode output





ANALOG PHASE SHIFTER FUNCTIONNAL BLOCK DIAGRAM

Typical Characteristics (ambiant 25°C on heat sink otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Comment
Positive supply voltage	VDD		7.6	8	8.4	V	
Negative supply voltage	VEE		-3.47	-3.3	-3.14	V	
Positive supply current	IDD		200	300	400	mA	
Negative supply current	IEE			6	10	mA	
Input frequency	F		9.95	10.709	11.5	GHz	Note 1
Input impedance adaptation	S11	50 Ohm		-13	-10	dB	
Output impedance adaptation	S22	50 Ohm		-11	-10	dB	
Input amplitude	Vin		300		1 000	mVpp	Note 2
Output amplitude max	Voutmax	With AGC	7			Vpp	
Output amplitude min	Voutmin	With AGC			2	Vpp	
AGC amplitude control voltage	Vagc	Vout and Vin from Min to Max	-2.0		0	V	
AGC gain slope	Sagc	Monotonic		100		mV/Vpp	
AGC input impedance	Zagc			1 000		Ohm	
Min output controlled phase delay	Ph delay	Vph from min to max	0		150	ps	Note 3
Phase delay control voltage	Vph		-2		-1.4	V	
Phase delay control slope	Sph			270		ps/V	Note 3
Vph input impedance	Zph			1 300		Ohm	
Second harmonic	H2			-30	-20	dB	
Third harmonic	H3				-30	dB	
Power detector output voltage	Vdet	Vout = Max Vout = Min	3.5		5.5	V	Note 3
Output voltage variation with phase delay control	Δ_{ph}Vout	Vph from Min to Max			2	dBpp	
Phase delay variation with temperature	Δ_TPh delay	Input and controls = constants		0.25	0.4	ps/°C	
Phase delay variation with gain control	Δ_GPh delay	Vout from Min to Max		5		ps	

Note 1 : phase shift frequency range is from 8GHz to 12GHz
Note 2 : input dynamic range to get output dynamic range from 2 to 7 Vpp
Note 3 : 11.1 GHz

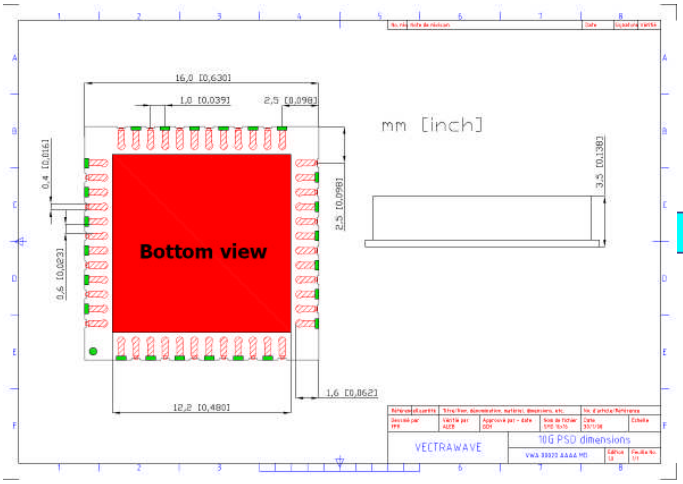
Environment Parameters		Symbols	Min	Max	Units
Operating temperature	Case (bottom)	T_{op}	-5	+75	°C
Storage temperature	Case (bottom)	T_{stg}	- 40	+85	°C

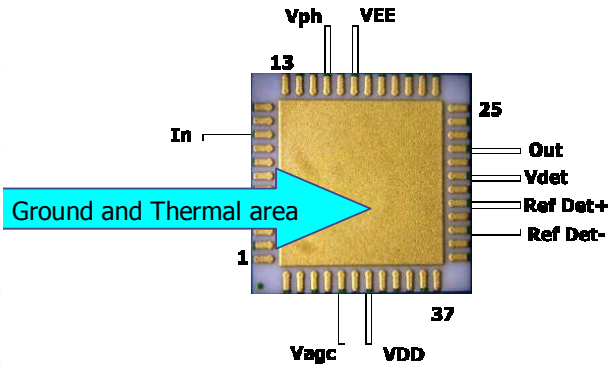
Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Positive supply voltage	VDD_{max}	0	+9	V
Negative supply voltage	VEE_{max}	-3.5	0	V
Storage temperature - Case (bottom)-	Tst		125	°C
Output controlled phase delay voltage command	Ph delay	VEE	VDD	V
Phase delay control voltage command	Vph	VEE	VDD	V

Pin out and pin description

Pad #	Function	Pad #	Function	Pad #	Function	Pad #	Function
1	Ground	13	Ground	25	Ground	37	Ground
2	Ground	14	Ground	26	Ground	38	Ground
3	Ground	15	Ground	27	Ground	39	Ground
4	Ground	16	Vph	28	Output	40	Ground
5	Ground	17	Ground	29	Ground	41	Ground
6	Ground	18	Vee	30	Vdet	42	Vdd
7	Ground	19	Ground	31	Ground	43	Ground
8	Ground	20	NC	32	Ref Det +	44	Vagc
9	Ground	21	Ground	33	Ground	45	Ground
10	Input	22	Ground	34	Ref Det -	46	Ground
11	Ground	23	Ground	35	Ground	47	Ground
12	Ground	24	Ground	36	Ground	48	Ground





Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **10G-PSD-7** module.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Bias On/Off procedures

Bias On	Bias Off
RF	Vdd
Vph	Vagc
Vee	Vee
Vagc	Vph
Vdd	RF

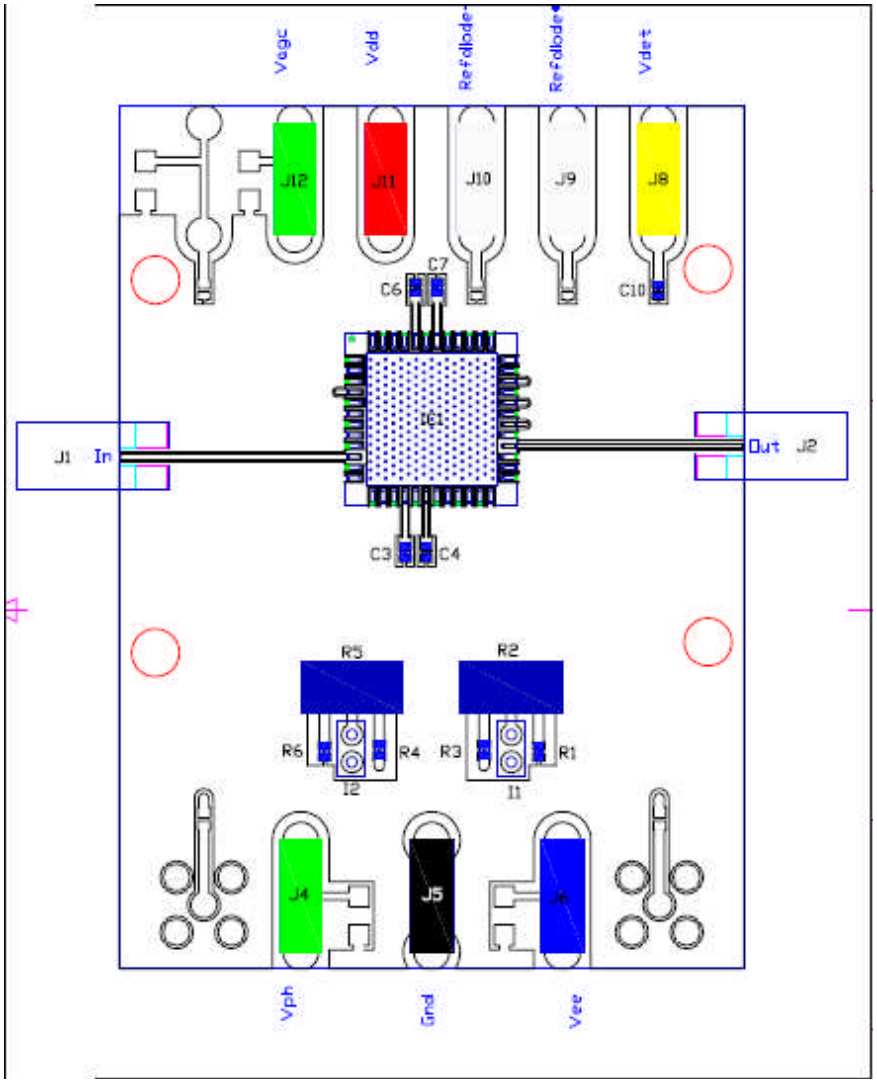
Ordering information

Product code	Name
VWA 00020 AB	10G-PSD-7 7V SMD Phase shifter
VWA 00039 AB	Demonstration board equipped w/phase shifter VWA 00020 AB
Other product variants are existing ➔ contact us	

xG-PSDx-DB	Demo-Board	VWA 00039Ax

Description

– The **xG-PSDx-DB** is a evaluation board for phase shifter driver in 16mm SMD package.

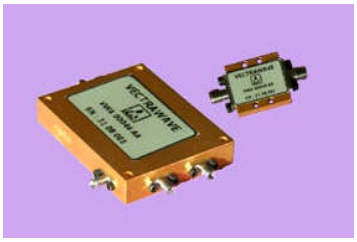


Lay out

Pin out when used with VWA 00020 Ax xx

Component	Type	SMD pin nb	Usage	Comment
J1	SMA	10	RF input	
J2	SMA	28	RF output	
J3	SMA	NA	J4 LF mod input	Not Connected
J4	DC connection	16	V phase command Vph	Direct command when I2 non connected
J5	DC connection	GND	GND	GND
J6	DC connection	18	Vee	
J7	SMA	NA	J12 LF mod input	Not Connected
J8	DC connection	30	Vdet	
J9	DC connection	32	Ref det +	Reference diode A
J10	DC connection	34	Ref Det -	Reference diode K
J11	DC connection	42	Vdd	
J12	DC connection	44	V gain control Vagc	Direct command when I1 non connected
J13	DC connection	NA	NA	Not Connected
I1	Strap		Allow Vagc adjustment via R2. Active when strap connected.	J12 must be not connected.
I2	Strap		Allow Vph adjustment via R5. Active when strap is connected	J4 must be not connected.
R2	Potentiometer		Allow Vagc adjustment	
R5	Potentiometer		Allow Vph adjustment	

Remove straps I1 and I2 for direct command of Vagc and Vph with J12 and J4 respectively.



VWA-10-PSMX-21-21-43

Clock Generator with integrated Phase Shifter @ 21.5GHz and 43GHz

Description

The **VWA-10-PSMX-21-21-43** is a clock speed doubler with phase shifter for high speed transmission at 43Gbps.

The **PSMX** module integrates two similar phase shifter and multiplier blocks in parallel, offering two outputs at the same frequency with adjustable relative phase.

The second multiplied (and phased) frequency is split into two paths; one is followed by a frequency doubler.

All the outputs are filtered by a band pass filter; specific frequency plan can be designed by selecting appropriate filters.

With an input frequency in the 10,7GHz window, the **PSMX** delivers two 21,5GHz signals and one 43Ghz signal. All the output signals are phase shifted with regards to the input, the second 21,5GHz and the 43GHz signal being phase shifted with regards to the first 21,5GHz output signal.

The phase shifters are digitally controlled with a 6 bits command.

Features

- Input frequency 10,7GHz
- Output frequencies 21,5GHz (2 outputs) and 43GHz
- Two independent phase shifters
- 6 bits phase shift command
- 5.6° phase shift step
- 50Ω RF Single ended input and output
- AC coupled
- K connector
- +5V & -5V supply voltage

Applications

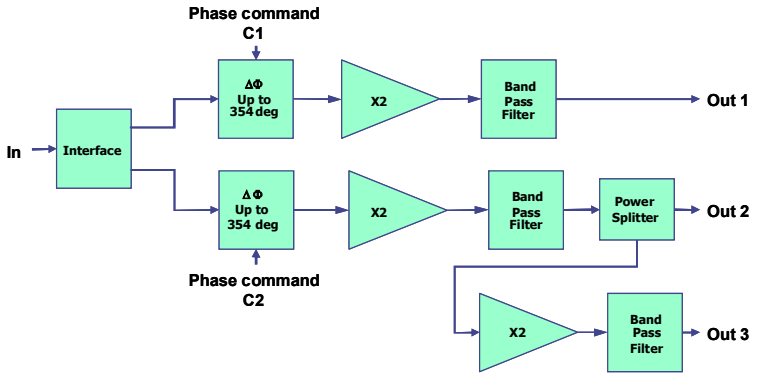
- SONET/SDH
- DPSK, DQPSK
- Clock Generation and Phase Matching
- 22Gb/s and 43Gb/s
- E2O driver
- Fiber transmission
- Broadband communication
- Test and measurement

Single clock doublers from 10.7 GHz to 21.5 GHz and from 21.5 GHz to 43 GHz also available

Ordering information:

VWA 00045 AD	Clock Generator with phase control for 21,5GHz	VWA 00047 AA	Clock Speed Doubler 21,5 GHz to 43 GHz with Filter
VWA 00054 AD	Clock Generator with phase control for 21,5GHz and 43GHz	VWA 00053 AA	Clock Speed Doubler 10,7GHz to 21,5 GHz with Filter

Functional Block Diagram

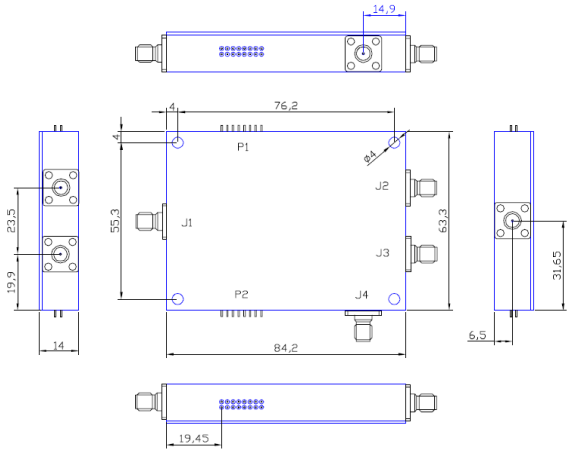


Typical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Comment
Positive supply voltage	VDD			5		V	
Negative supply voltage	VEE			-5		V	
Positive supply current	IDD			300		mA	
Negative supply current	IEE			20		mA	
Input level J1	Pin			10		dBm	
Output level J2	Pout 1			10		dBm	
Output level J3	Pout 2			7		dBm	
Output level J4	Pout 3			12		dBm	
Output Impedance matching	S22	J2, J3, J4		15		dB	
Input Impedance matching	S11	J1		8		dB	

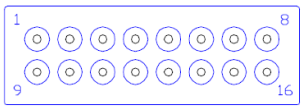
Mechanical dimensions and pin out

VWA 00054 AD



Connecteurs vidéo P1 & P2 :

Affectation des perles



1 : NC	9 : NC
2 : NC	10 : NC
3 : NC	11 : NC
4 : GND	12 : GND
5 : BIT5	13 : BIT6
6 : -5V	14 : BIT4
7 : BIT2	15 : BIT3
8 : +5V	16 : BIT1

NB : Vue extérieure du boîtier.

Les 2 connecteurs ont un brochage identique.

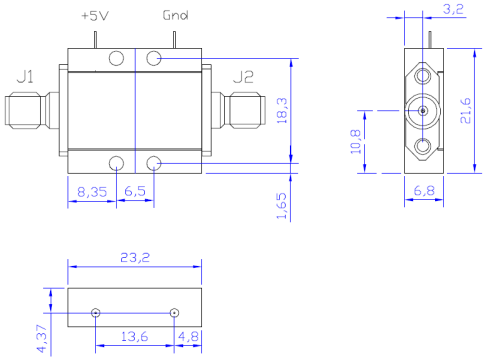
Table de Vérité :

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Phase
0	0	0	0	0	0	Ref.
+5V	0	0	0	0	0	5.625
0	+5V	0	0	0	0	11.25
0	0	+5V	0	0	0	22.5
0	0	0	+5V	0	0	45.0
0	0	0	0	+5V	0	90.0
0	0	0	0	0	+5V	180.0
+5V	+5V	+5V	+5V	+5V	+5V	360.0

Accès HF :

J1 :	Entrée 10.75 GHz	Niveau : + 10 dBm
J2 :	Sortie 21.5 GHz	Niveau : + 10 dBm
J3 :	Sortie 21.5 GHz	Niveau : + 7 dBm
J4 :	Sortie 43 GHz	Niveau : + 12 dBm

VWA 00047 AA & VWA 00053 AA



Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **PSMX**.

VWA 00060 AB xx DS Rev 0.1

20G-PSDD-4

20G phase shifter with integrated Doubler & Driver

Description

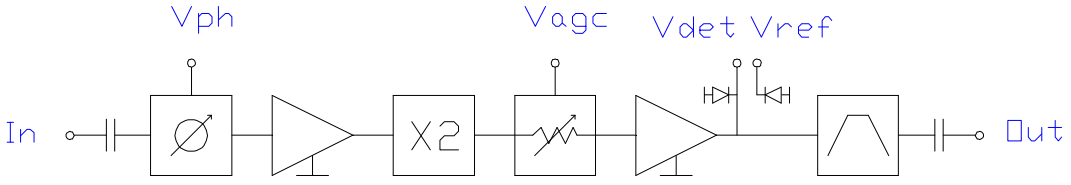
The **20G-PSDD-4** is an analog phase shifter with integrated frequency doubler and variable gain stage with output power amplifier in SMD package.
For an input frequency of 10,7GHz the device delivers an output signal at 21,4 GHz.
The device is capable of up to 800° phase shift. The output amplifier is designed to deliver 4Vpp with low distortion (also included output a filter). The variable gain stage has a wide dynamic range of 18dB.
A power detector, with reference diode, is also included, giving a direct measurement of the output power.

Features

- 16x16 mm² SMD
- 48 pins w/1mm pitch
- 50Ω RF Single ended input and output
- RF input and output are AC coupled
- Input frequency band : 9.9 – 11.5 GHz
- Output frequency band : 19.8 – 23 GHz
- Wide phase shift from 0 to >540°(up to 800°)
- Low power
- +9V and 5V voltage supply
- Output level, up to 4Vpp
- Wide dynamic gain control 18dB
- Phase shift command
- Gain command
- Output level detection
- Ref diode output

Applications

- Phase control
- Radar
- Fiber transmission
- DPSK
- 20GBps, 40GBps



ANALOG PHASE SHIFTER DOUBLER FUNCTIONNAL BLOCK DIAGRAM

Typical Characteristics (ambiant 25°C on heat sink otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Comment
Positive supply voltage 1	VDD1		8.55	9	9.45	V	
Positive supply voltage 2	VDD2		8.55	9	9.45	V	
Positive supply voltage 3	Vcc		4.75	5	5.25	V	
Positive supply current 1	IDD1	VDD1	150	200	250	mA	
Positive supply current 2	IDD2	VDD2	150	200	250	mA	
Positive supply current 3	Icc	Vcc		100	120	mA	
Input frequency	F		9.95	10.709	11.5	GHz	
Input impedance adaptation	S11	50 Ohm			-10	dB	
Output impedance adaptation	S22	50 Ohm			-8	dB	
Input amplitude	Vin		300		1 000	mVpp	
Output amplitude max	Voutmax	With AGC	4			Vpp	
AGC amplitude control voltage	Vagc	Vout and Vin from Min to Max	-4		4	V	
AGC gain slope	Sagc	Monotonic				Vpp/V	TBD
AGC input impedance	Zagc					Ohm	TBD
Min Max output controlled phase delay	Ph delay Max	Vph=10V @ 21.4 GHz	60	90		ps	
Phase delay control voltage	Vph		0		10	V	
Phase delay control slope	Sph			9		ps/V	
Vph input impedance	Zph					Ohm	TBD
Input signal at output	H0	10.7 GHz		-30	-20	dB	
Third harmonic	H3	32.1 GHz		-30	-20	dB	
Power detector output voltage	Vdet	Vout = Max		500		mV	TBC
Output voltage variation with phase delay control	ΔVout(Δ_{ph})	Vph from Min to Max				dBpp	TBD
Phase delay variation with temperature	ΔPh delay(Δ_T)	Input and controls = constants				ps/°C	TBD
Phase delay variation with gain control	ΔPhdelay(Δ_G)	Vout from Min to Max				ps	TBD

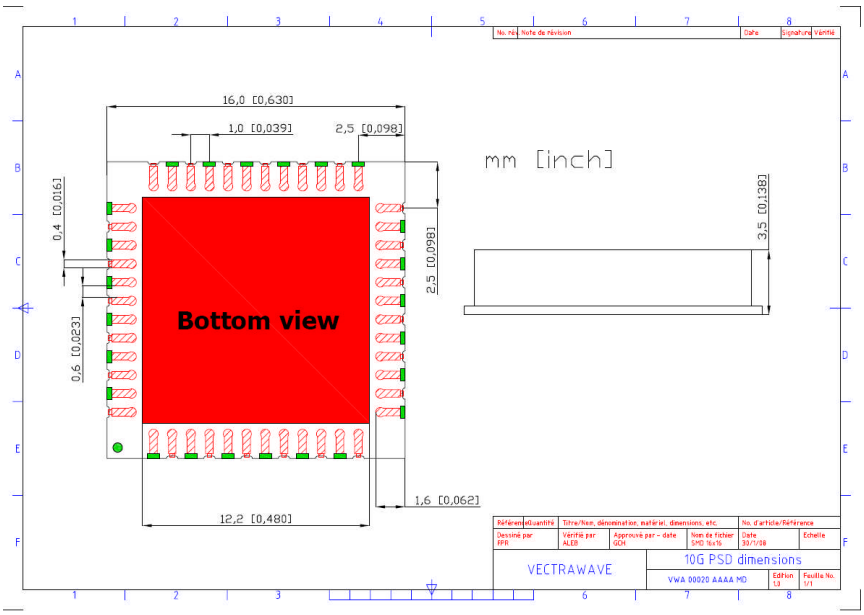
Environment Parameters		Symbols	Min	Max	Units
Operating temperature	Case (bottom)	T_{op}	-5	+75	°C
Storage temperature	Case (bottom)	T_{stg}	- 40	+85	°C

Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Positive supply voltage 1,2	VDD_{max}		+10	V
Positive supply voltage 3	Vcc_{max}		+6	V
Storage temperature - Case (bottom)-	Tst_{max}		125	°C
Phase delay control voltage command	Vph_{max}		+11	V
AGC amplitude control voltage	$Vagc_{max}$	-6	+6	V

Pin out and pin description

Pad #	Function	Pad #	Function	Pad #	Function	Pad #	Function
1	Ground	13	Ground	25	Ground	37	Ground
2	Ground	14	Ground	26	Ground	38	Ground
3	Ground	15	Ground	27	Ground	39	Ground
4	Vdd1	16	Vph	28	Output	40	Ground
5	Ground	17	Ground	29	Ground	41	Ground
6	Ground	18	NC	30	Vdd2	42	Vagc
7	Ground	19	Ground	31	Ground	43	Ground
8	Ground	20	NC	32	Vdet	44	Vcc
9	Ground	21	Ground	33	Ground	45	Ground
10	Input	22	Ground	34	Vref	46	Ground
11	Ground	23	Ground	35	Ground	47	Ground
12	Ground	24	Ground	36	Ground	48	Ground



Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **20G-PSDD-4** modules.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Product code	Name
VWA 00060 AB	20G-PSDD-4 SMD 540°Phase shifter
VWA 00061 AB	Demonstration board equipped w/phase shifter VWA 00060 AA

VWA 00066 AA xx DS Rev 0.2

preliminary

20G-PSDD-8

20G phase shifter with integrated Doubler & Driver

Description

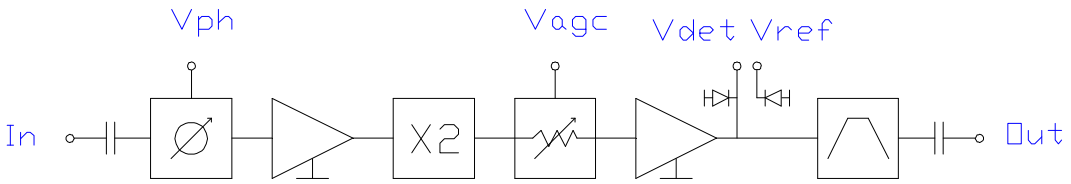
The **20G-PSDD-8** is an analog phase shifter with integrated frequency doubler and variable gain stage with output power amplifier in SMD package.
For an input frequency of 10,7GHz the device delivers an output signal at 21,4 GHz.
The device is capable of up to 600° phase shift at 10GHz. The output amplifier is designed to deliver up to 8Vpp with low distortion (also included output a filter). The variable gain stage has a wide dynamic range of 20dB.
A power detector, with reference diode, is also included, giving a direct measurement of the output power.

Features

- 16x16 mm² SMD
- 48 pins w/1mm pitch
- 50Ω RF Single ended input and output
- RF input and output are AC coupled
- Input frequency band : 9.9 – 11.5 GHz
- Output frequency band : 19.8 – 23 GHz
- Wide phase shift >360°(up to 600°) at 10GHz
- Low power < 3.5W
- +/-5V voltage supplies
- Output level, up to 8Vpp
- Wide dynamic gain control 20dB
- Phase shift command
- Gain command
- Output level detection
- Ref diode output

Applications

- Phase control
- Radar
- Fiber transmission
- DPSK
- 20GBps, 40GBps



ANALOG PHASE SHIFTER DOUBLER FUNCTIONNAL BLOCK DIAGRAM

Typical Characteristics (ambiant 25°C on heat sink otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Comment
Positive supply voltage 1	Vcc1		4.75	5	5.25	V	
Positive supply voltage 2	Vcc2		4.75	5	5.25	V	Output amp
Negative supply voltage 1	Vee		-5.46	-5.2	-4.95	V	
Positive supply current 1	Icc1	Vcc1		140	185	mA	
Positive supply current 2	Icc2	Vcc2		250	300	mA	
Negative supply current 1	Iee	Vee			1	mA	
Input frequency	F		9.95	10.709	11.5	GHz	
Input impedance adaptation	S11	50 Ohm			-10	dB	
Output impedance adaptation	S22	50 Ohm			-8	dB	
Input amplitude	Vin		300		1 000	mVpp	
Output amplitude min	Voutmin	With AGC			2	Vpp	
Output amplitude max	Voutmax	With AGC	8			Vpp	
AGC amplitude control voltage	Vagc1,2	Vout and Vin from Min to Max	-5		0	V	
AGC modulation bandwidth	AGC_{BW}	Vagc1,2	10			kHz	
AGC gain slope	Sagc	Monotonic		6		dB/V	Note 1
AGC input current	Iagc	Vagc1,2			100	µA	Note 2
Minimum Max output controlled phase delay	Ph delay Max	Vph=5V @ Fout=21.4 GHz	155			ps	
Phase delay control voltage	Vph		0		5	V	
Phase delay modulation Bandwidth	Vph_{BW}		10			kHz	
Phase delay control slope	Sph	Monotonic		30		ps/V	
Vph input current	Iph				100	µA	Note 3
Input signal at output	H0	10.7 GHz		-30	-20	dB	
Third harmonic	H3	32.1 GHz		-30	-20	dB	
Power detector output voltage	Vdet-Vref	Vout = 4Vpp		400		mV/Vpp	Note 4
Output voltage variation with phase delay control	$\Delta Vout(\Delta_{ph})$	Vph from Min to Max			1	dBpp	
Phase delay variation with temperature	$\Delta Ph\ delay(\Delta_T)$	Input and controls = constants			0.5	ps/°C	
Phase delay variation with gain control	$\Delta Phdelay(\Delta_G)$	Vout from Min to Max			5	ps	

Note1 : Vagc1 and Vagc2 average. Min and max to be confirmed
Note2: input command is a MESFET grid. Max current to be confirmed
Note3: input command equivalent circuit is a series connected diode and resistor.
Note4: Vdet-Vref monotonic with output power.

Environment Parameters

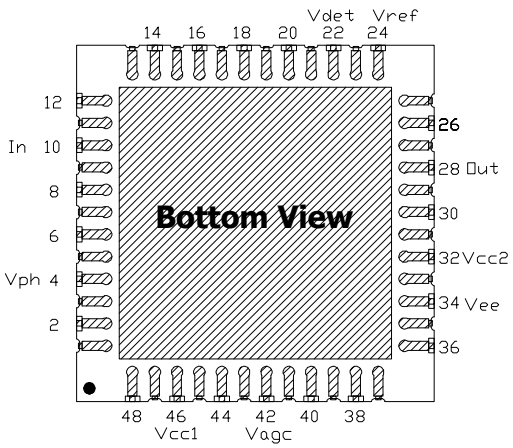
Environment Parameters		Symbols	Min	Max	Units
Operating temperature	Case (bottom)	T_{op}	-5	+75	°C
Storage temperature	Case (bottom)	T_{stg}	- 40	+85	°C

Absolute maximum ratings

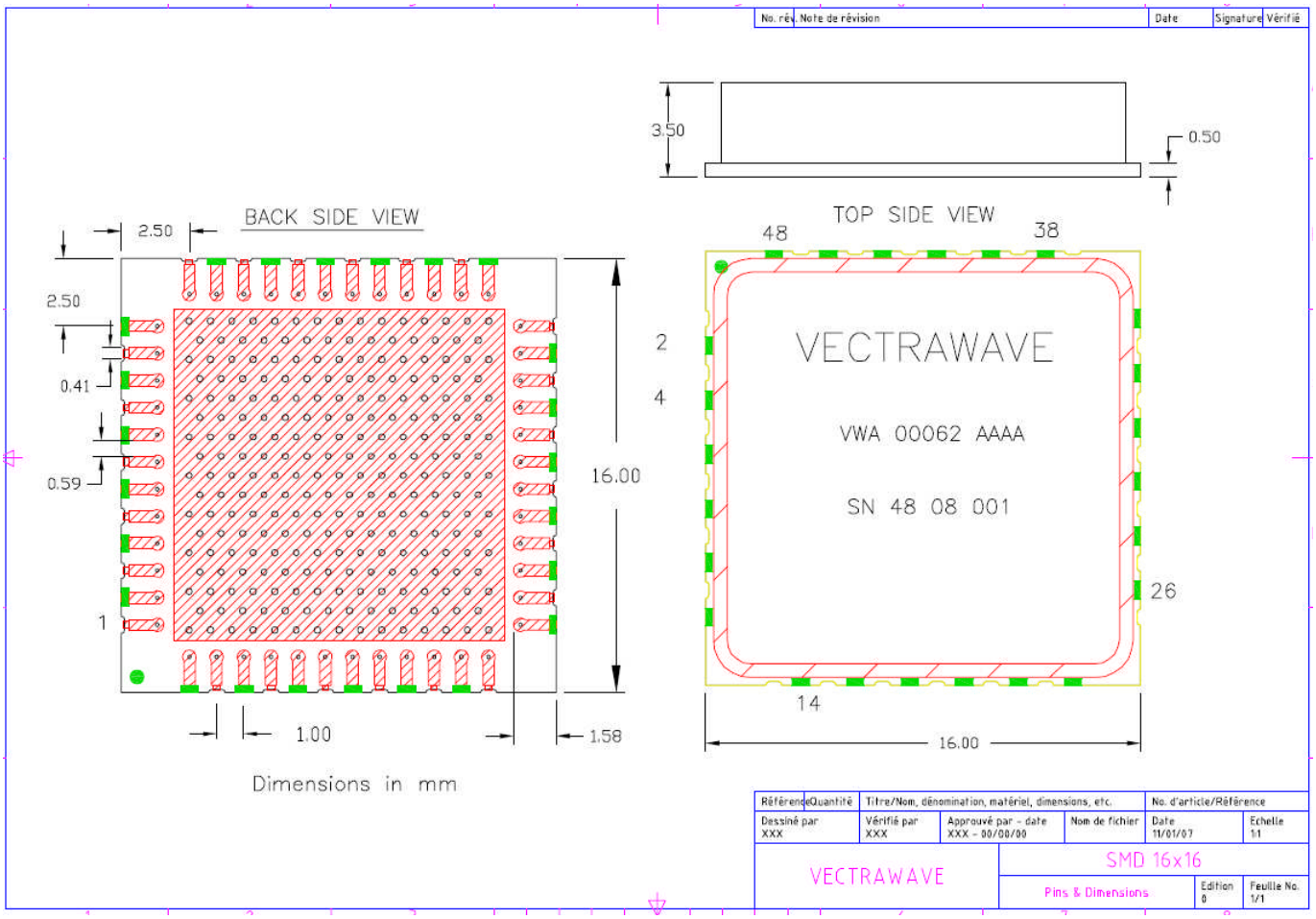
Maximum ratings	Symbols	Min	Max	Units
Positive supply voltage 1,2	Vcc_{max}		+6	V
Storage temperature	Tst_{max}		125	°C
Phase delay control voltage command	Vph_{max}	-1	+8	V
AGC amplitude control voltage	$Vagc_{max}$	-6	+6	V

Pin out and pin description

Pad #	Function	Pad #	Function	Pad #	Function	Pad #	Function
1	Ground	**13**	Ground	**25**	Ground	**37**	Ground
2	Ground	**14**	Ground	**26**	Ground	**38**	Ground
3	Ground	**15**	Ground	**27**	Ground	**39**	Ground
4	Vph	**16**	Ground	**28**	Output	**40**	Ground
5	Ground	**17**	Ground	**29**	Ground	**41**	Ground
6	Ground	**18**	Ground	**30**	Ground	**42**	Vagc
7	Ground	**19**	Ground	**31**	Ground	**43**	Ground
8	Ground	**20**	Ground	***32***	Vcc2	**44**	Ground
9	Ground	**21**	Ground	**33**	Ground	**45**	Ground
10	Input	**22**	*Vdet*	***34***	Vee	**46**	Vcc1
11	Ground	**23**	Ground	**35**	Ground	**47**	Ground
12	Ground	**24**	*Vref*	**36**	Ground	**48**	Ground



Mechanical dimensions



Handling This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **20G-PSDD-8** modules.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

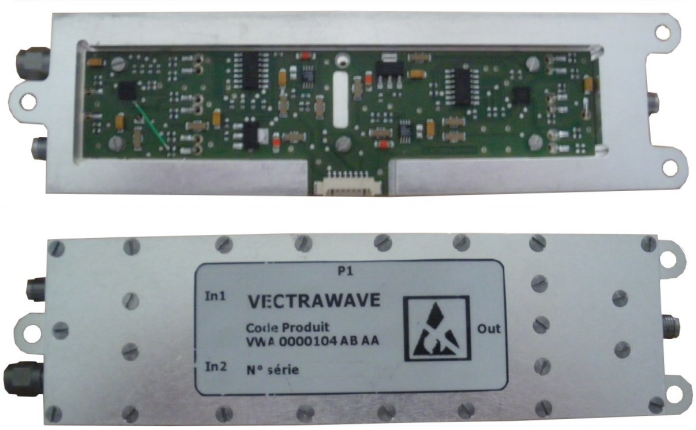
Ordering information

Product code	Name
VWA 00066 AA	20G-PSDD-8 SMD 600°Phase shifter
VWA 00064 AB	Demonstration board equipped w/phase shifter VWA 00066 AA

Bias On/Off procedures

Bias On	Bias Off
Vee	RF
Vph	Vcc2
	Vcc1
Vagc	
Vcc1	Vagc
Vcc2	Vph
RF	Vee

Data Sheet **MCM Product-Line**



Multi-chip Module

X to Ka band Filters Bank

Description

- Switched filter banks
- This module allows to choose one filter among four
- The gain (thermal compensated) is adjustable filter by filter
- It is possible to choose one input among two
- The module integrates all the RF passives and biasing devices in the same package

Main Features

- K connectors
- Applications over X and Ka frequency range
- Independent gain adjustment for each filter
- Thermal compensation inside
- Bias regulation inside
- TTL compatible control

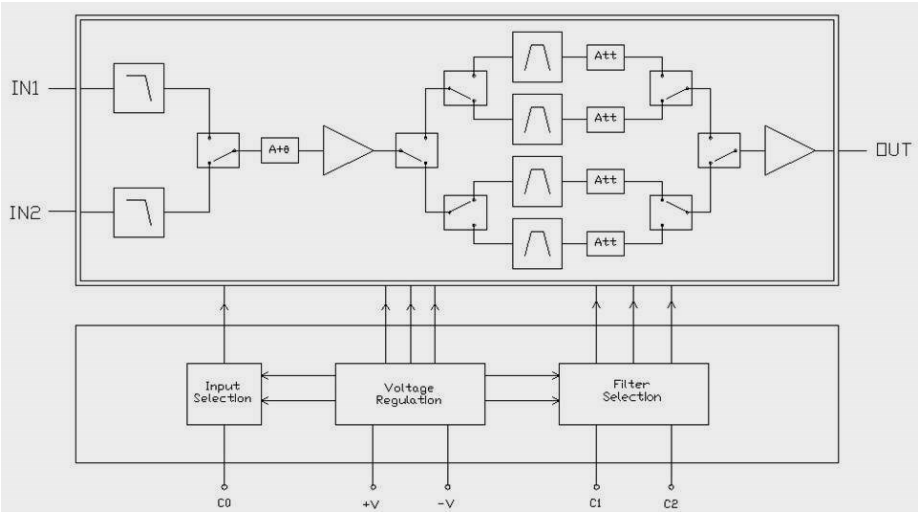
Applications

- Commercial and Military Radar
- Electronic Warfare

Ordering Information

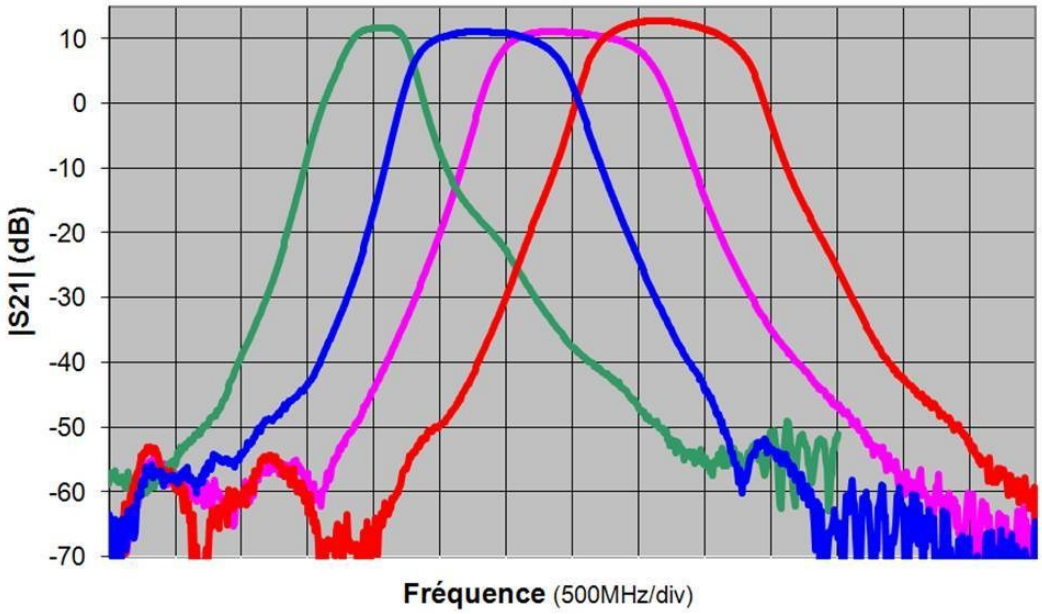
- P/N VWA 0000104 ABAA for detailed unit
- Contact us for specific request

Functional Block Diagram

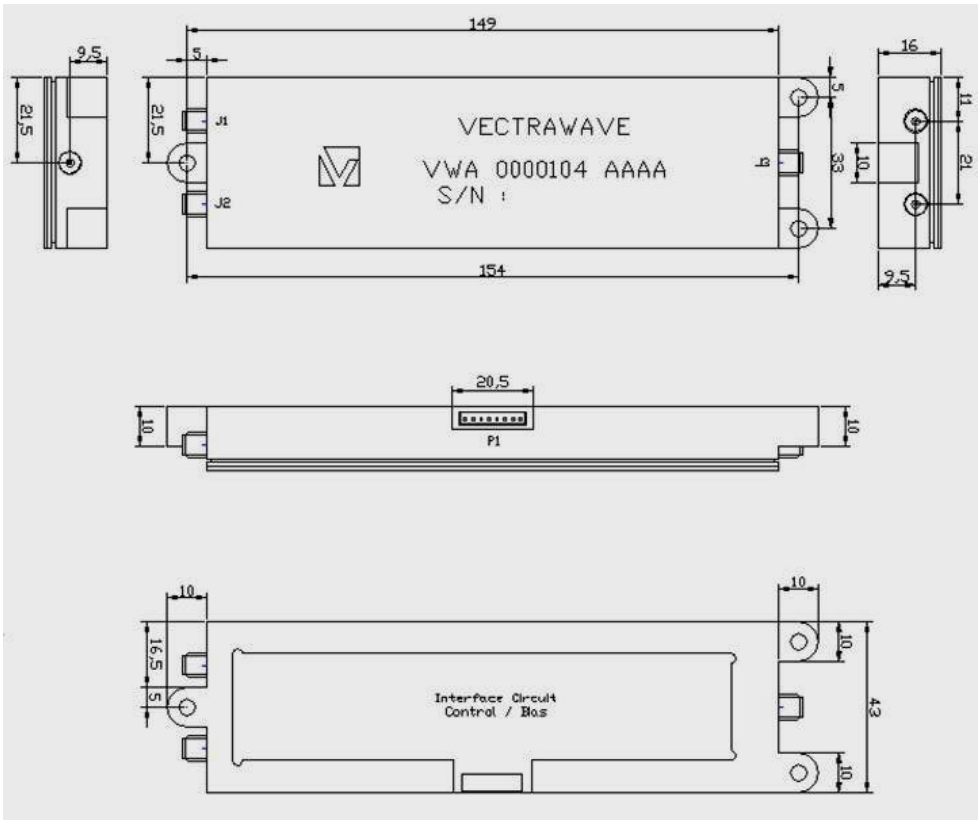


Data Sheet **MCM Product-Line**

X-band Application Example



Mechanical Dimensions



Product family: VWA-15-VA-257

5 Gb/s, 10,7 Gb/s RZ & 12,5 Gb/s NRZ
Driver Amplifier with 6 to 8 Vpp Output control
for LiNbO3 (LN)
and Electro Absorption (EA) Modulators

Description

The **VWA-15-VA-257** is a broadband dual stage GaAs MMIC amplifier module, which provides up to 25 dB gain from 55 kHz to 15 GHz and delivers +21 dBm of output power, with a single Voltage regulated Bias. The output voltage can be set between 4 to 8 V_{pp} in varying the Pin V_{ctl}.

Features

- Very Low Jitter
- Very Low rise and fall time (bellow 17ps)
- Output V_{pp} control
- Ultra Wideband
- Very High Gain
- Medium power
- 50 Ohm impedance
- Single +12V supply

Applications

Main applications include: Long Haul, Medium Haul, Metro Access, Test Bench, Test & Measurement.
This unit performs LN and EAM driver functions for 10.7 Gb/s RZ data rates and 2.5 Gb/s, 5 Gb/s, 9,958 Gb/s and from 10,7 Gb/s to 12.5 Gb/s for NRZ data rates. The driver amplifier has single-ended input and output, and SMA field replaceable RF connectors (male or female

Typical Characteristics (25°C)

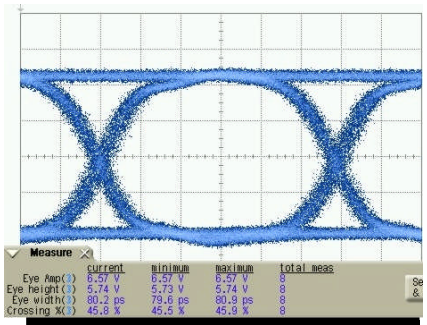
Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	15			GHz
Low Frequency Response (-3 dB)	BW_{Low}			55	kHz
Averaged Gain	G	25			dB
Input Return Loss (1 GHz–12 GHz)	S11		- 8		dB
Output Return Loss (1 GHz–12 GHz)	S22		-8		dB
Output Voltage max	$V_{pp\text{-}max}$	7	8		V
Output voltage control command	V_c	0		1,5	V
Bias Voltage	V_{bias}	+10	+12	+ 15	V
Power Dissipation	P		3,5		W
RMS Jitter (including E/O modulator)	RMS Jitter			2	ps

Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-5		+70	°C
Storage temperature	T_{stg}	-40		+85	°C

Absolute maximum ratings

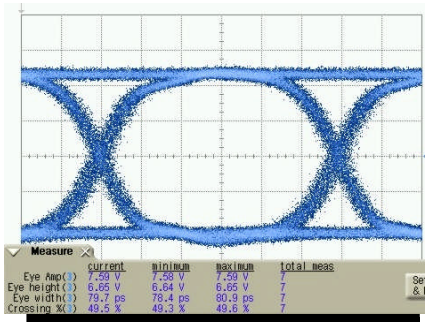
Maximum ratings	Symbols	Min	Typ	Max	Units
Supply Voltage	$V_{bias\ max}$			+15	V
Lead soldering temperature				250	°C

Typical Eye diagram:

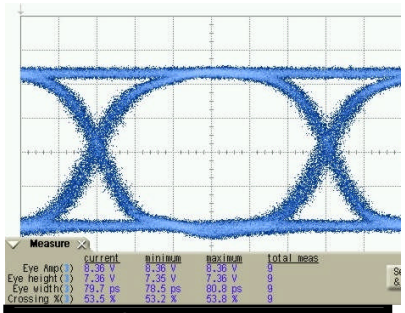


DATA OUT Measurements		
Vc =	0,29	V
Ibias	273,0	mA
Eye Amplitude:	6,57	Vpp
Eye Height:	5,74	Vpp
Eye Width:	80,3	ps
Rise Time:	28,0	ps
Fall Time:	30,6	ps
Jitter RMS:	2,4	ps
Jitter pp:	12,1	ps
Crossing %:	45,7	%
Jitter DRIVER		
Jitter RMS:	0,7	ps
Jitter pp:	3,9	ps

Data Out

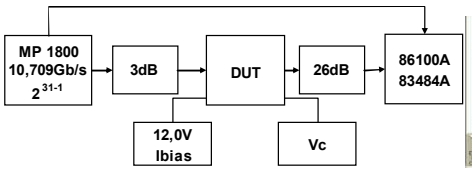


DATA OUT Measurements		
Vc =	1,69	V
Ibias	293,0	mA
Eye Amplitude:	7,58	Vpp
Eye Height:	6,64	Vpp
Eye Width:	79,7	ps
Rise Time:	32,8	ps
Fall Time:	30,2	ps
Jitter RMS:	2,5	ps
Jitter pp:	12,4	ps
Crossing %:	49,5	%
Jitter DRIVER		
Jitter RMS:	0,5	ps
Jitter pp:	4,8	ps

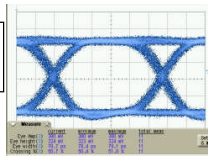


DATA OUT Measurements		
Vc =	3,00	V
Ibias	309,0	mA
Eye Amplitude:	8,36	Vpp
Eye Height:	7,36	Vpp
Eye Width:	79,6	ps
Rise Time:	34,5	ps
Fall Time:	30,0	ps
Jitter RMS:	2,4	ps
Jitter pp:	11,7	ps
Crossing %:	53,4	%
Jitter DRIVER		
Jitter RMS:	0,5	ps
Jitter pp:	2,1	ps

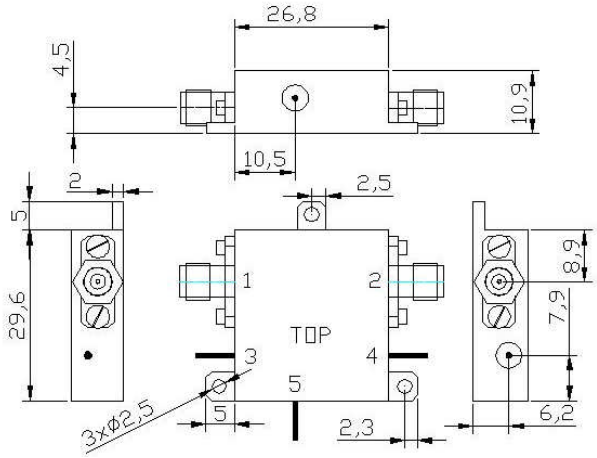
Test Set



Data In



Mechanical characteristics



Pin Out

Pin Nb	Designation
1	Input
2	Output
3	Vbias
4	Ground
5	V_c

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-15-VA-257** module.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

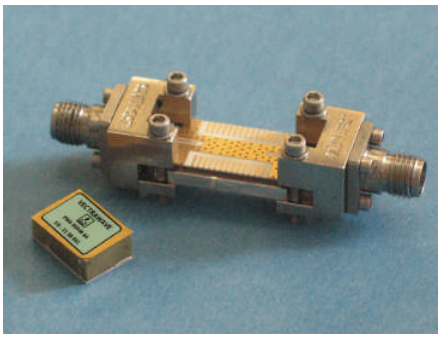
Part number	Operating temp. °C	Connector In	Connector Out
VWA 00022 AA	-5 / + 70	SMA female	SMA female
VWA 00022 AB	-5 / + 70	SMA female	SMA male
VWA 00022 AC	-5 / + 70	SMA male	SMA female
VWA 00022 AD	-5 / + 70	SMA male	SMA male

Options on demand:

- Other packages upon request
- Heat sink

High Speed Communication, Data drivers : VWA 00085 AA 1/2

VWA 00085 AAxx DS Rev 0.2



SMD Driver
VWA-23-D-7-SM

23Gbps 7V

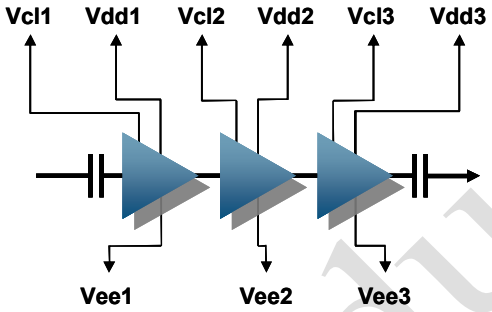
Description

The **VWA 00085 AA** is a Surface Mount amplifier for driving Lithium Niobat MZ double modulator up to 28Gbps.

The module integrates a triple stage amplifier with output level and cross point control commands. Output voltage can be adjusted from 7Vpp (eye amplitude opening) to 3Vpp or less without cross point change.

The module integrates all the passives devices in the same package.

Functional Block Diagram



Ordering information

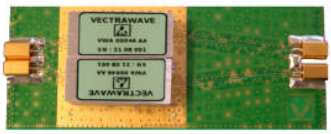
Part Number: VWA 00085 AA

Main Features

- Data rate up to 23Gb/s
- 7Vpp eye opening
- Input amplitude: 350mV pp
- Independent Output level and cross point adjustment
- SMD
- Low power consumption 2.9W

Applications

- D(Q)PSK
- 23 , 40 and 100Gbps



Typical Characteristics

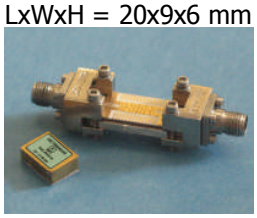
Electrical Parameters	Symbols	Min	Typ	Max	Units
High Frequency Response (-3 dB)	BW_{high}	20			GHz
Low Frequency Response (-3 dB)	BW_{Low}			50	kHz
Averaged max small signal gain	G	25	30		dB
Output Voltage max	$V_{pp\text{-}max}$	7	8		V
Output voltage control dynamic	ΔVout	3			dB
Rise time (20/80%)	Tr			12	ps
Fall time (20/80%)	Tf			12	ps
Added RMS Jitter	RMS Jitter			0,5	ps

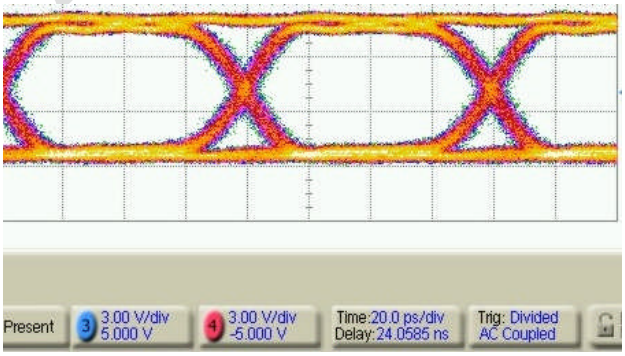
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature	T_{op}	-5		+75	°C
Storage temperature	T_{stg}	-40		+85	°C

Power supply	Symbols	Min	Typ	Max	Units
Positive supply voltage 1	Vdd1		8		V
Positive supply current 1	Idd1		90		mA
Positive supply voltage 2	Vdd2		8		V
Positive supply current 2	Idd2		90		mA
Positive supply voltage 3	Vdd3		8		V
Positive supply current 3	Idd3		200		mA
Control voltage 1	Vcl1				V
Control current 1	Icl1				mA
Control voltage 2	Vcl2				V
Control current 2	Icl2				mA
Control voltage 3	Vcl3				V
Control current 3	Icl3				mA
Negative supply voltage 1	Vee1				V
Negative supply current 1	Iee1				mA
Negative supply voltage 2	Vee2				V
Negative supply current 2	Iee2				mA
Negative supply voltage 3	Vee3				V
Negative supply current 3	Iee3				mA

Mechanical dimensions (mm) :

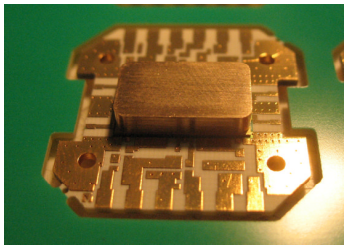
LxWxH = 20x9x6 mm





Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the device.



32 Gbps 7 Vpp Output Double Driver in SMD package

30kHz – 25GHz

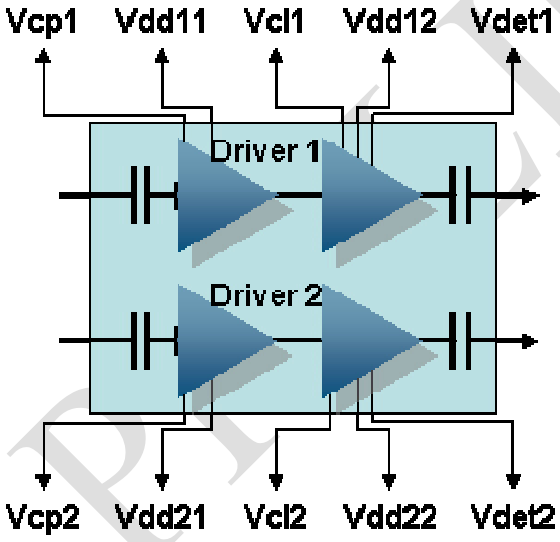
Description

The **VWA 00090 AA** is a double amplifier for driving Lithium Niobat MZ double modulator up to 32Gbps.

The module integrates two Double stage amplifiers with output level and cross point control commands. Output voltage can be adjusted from 2Vpp (eye amplitude opening) to 7Vpp or less without cross point change.

The module integrates all the RF passives and biasing devices in the same package, only low frequency coils are required on user board.

Functional Block Diagram



Ordering information

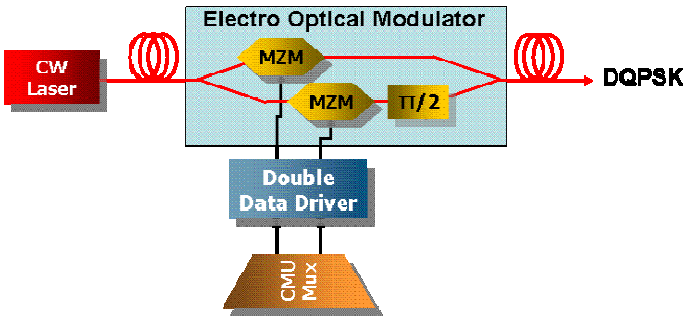
Code: VWA 00090 AA

Main Features

- SMD
- Small size 7x12,5x2,8 mm
- Data rate up to 32Gb/s
- Output voltage adjustable from 2Vpp to 7Vpp
- Input amplitude: ⩾350mV pp
- Cross point adjustment range 30% to 70%
- Independent Output level and cross point adjustment
- Integrated output level peak detector
- Power supply (typ): Vdd: +5V and +8V; -2V<Vg<+2V.
- Low power consumption <4W (Vout=7Vpp)

Applications

- DPSK
- DQPSK
- DP-QPSK
- 40 and 100Gbps



Typical Characteristics

Dynamic characteristics are given for:

- driver 1: Vdd11=5V, Vdd12=8V, -4V≤Vcl1≤1V, -0.5V≤Vcp1≤0V
- driver 2: Vdd21=5V, Vdd22=8V, -4V≤Vcl2≤1V, -0.5V≤Vcp2≤0V
- Input voltage = 500mVpp
- Bit rate 21.5Gbps

Electrical Parameters	Symbols	Min	Typ	Max	Units	Notes
High Frequency Response (-3 dB)	BW_{high}	25			GHz	
Low Frequency Response (-3 dB)	BW_{Low}			30	kHz	
Averaged max small signal gain	G	25	30		dB	
Input and output return loss	Sii			-10	dB	
Output Voltage max	$V_{pp\text{-}max}$	7	8	9	Vpp	
Output voltage control dynamic	ΔVout	3	5		dB	1
Rise time (20/80%)	tr		12	13	ps	2
Fall time (20/80%)	tf		11	13	ps	2
Added RMS Jitter	RMS Jitter			0.5	ps	
Differential phase (Amp1/Amp2)	ΔΦ12			2	ps	3
Differential gain (Amp1/Amp2)	ΔG12			1	dB	3
Crosstalk (Amp1 ⇔ Amp2)	Xtlk	30			dB	2
Output voltage control	Vcli	-4		1	V	5
Cross point voltage control	Vcpi	-0.3	-0.15	0	V	
Cross point variation with Vcli	Δ Cp		4	5	%	1
Output voltage detector	Vdet_i		37		mV/Vpp	4

Notes:

1. Vcl_i Min ≤Vcl_i ≤ Vcl_i Max
2. for Vout = 7Vpp
3. measured at 21.5 Gbps
4. measured at 21.5Gbps
5. apply through 1KOhm serial resistor

Power supply	Symbols	Min	Typ	Max	Units	Notes
First stage supply voltage	Vdd_i1	5	8	9	V	
First stage supply current	Idd_i1		110	120	mA	
Second stage supply voltage	Vdd_i2	8	8	9	V	
Second stage supply current	Idd_i2		180	210	mA	
Total power consumption driver1 & driver2	P	3.8	4		W	6

Notes:

6. Output voltage = 7Vpp

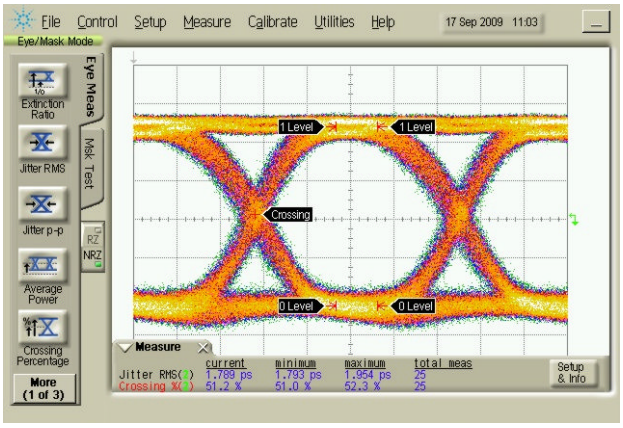
Environment Parameters	Symbols	Min	Typ	Max	Units
Operating temperature (case)	T_{op}	-5		+75	°C

Absolute Maximum ratings

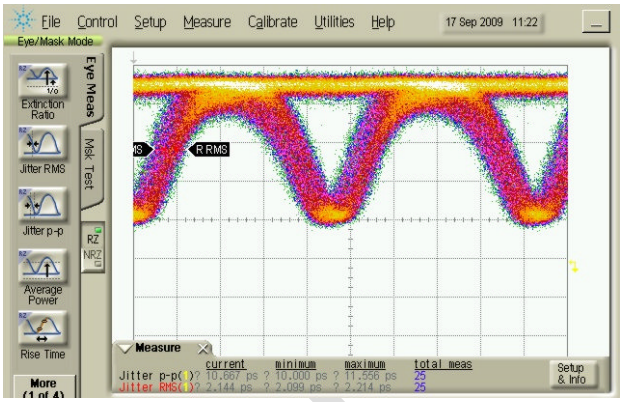
Environment Parameters	Symbols	Min	Typ	Max	Units
Storage temperature	T_{stg}	-40		+125	°C

Power supply	Symbols	Min	Typ	Max	Units
First stage supply voltage	Vdd_i1 Max	0		10	V
Second stage supply voltage	Vdd_i2 Max	0		10	V
Output voltage control	Vcli Max	-5		4	V
Cross point voltage control	Vcpi Max	-2.5		0	V

Typical measurements

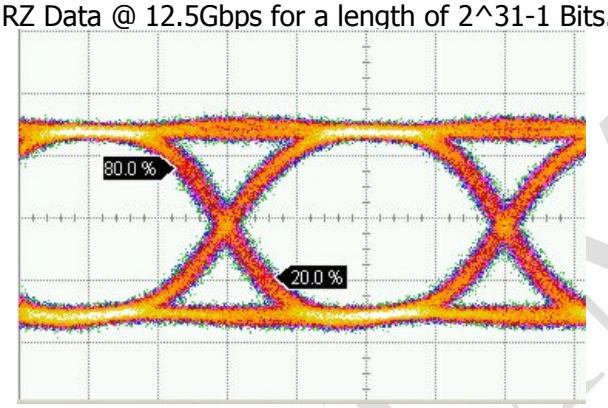


21.5Gbps electrical 7Vpp eye amp diagram

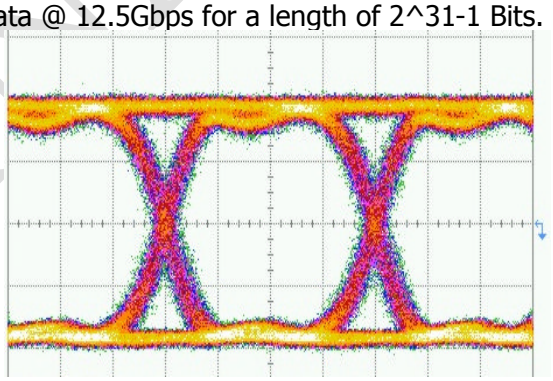


21.5Gbps DPSK optical eye diagram

NRZ Data @ 12.5Gbps for a length of 2^31-1 Bits.



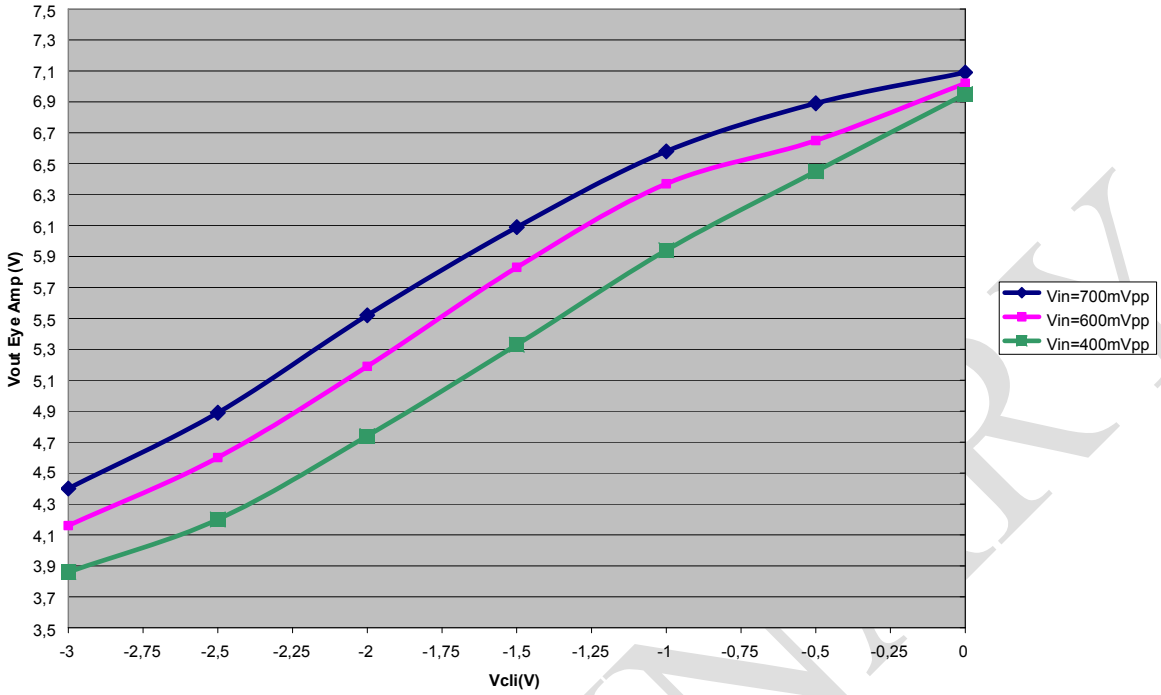
NRZ Data @ 12.5Gbps for a length of 2^31-1 Bits.



Input signal			
Cp (%)	**tr (ps)**	**tf (ps)**	**Eye Amp (Vpp)**
49	25.3	22.6	0.593

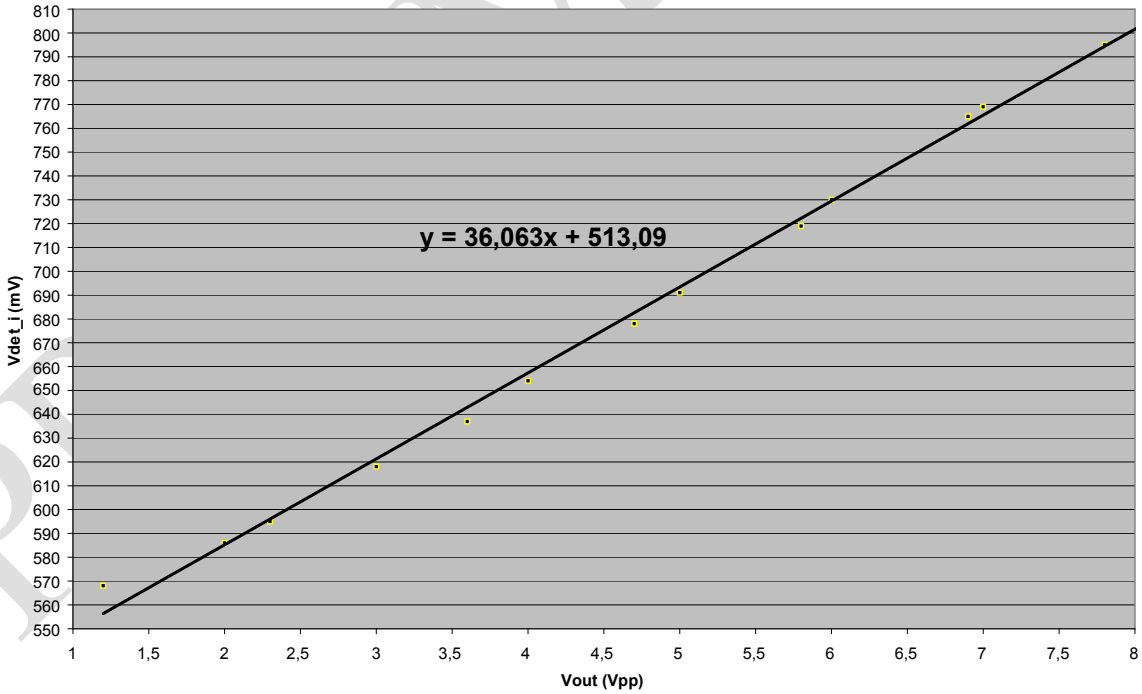
Output signal			
Cp (%)	**tr (ps)**	**tf (ps)**	**Eye Amp (Vpp)**
50.6	16	16.4	7.1

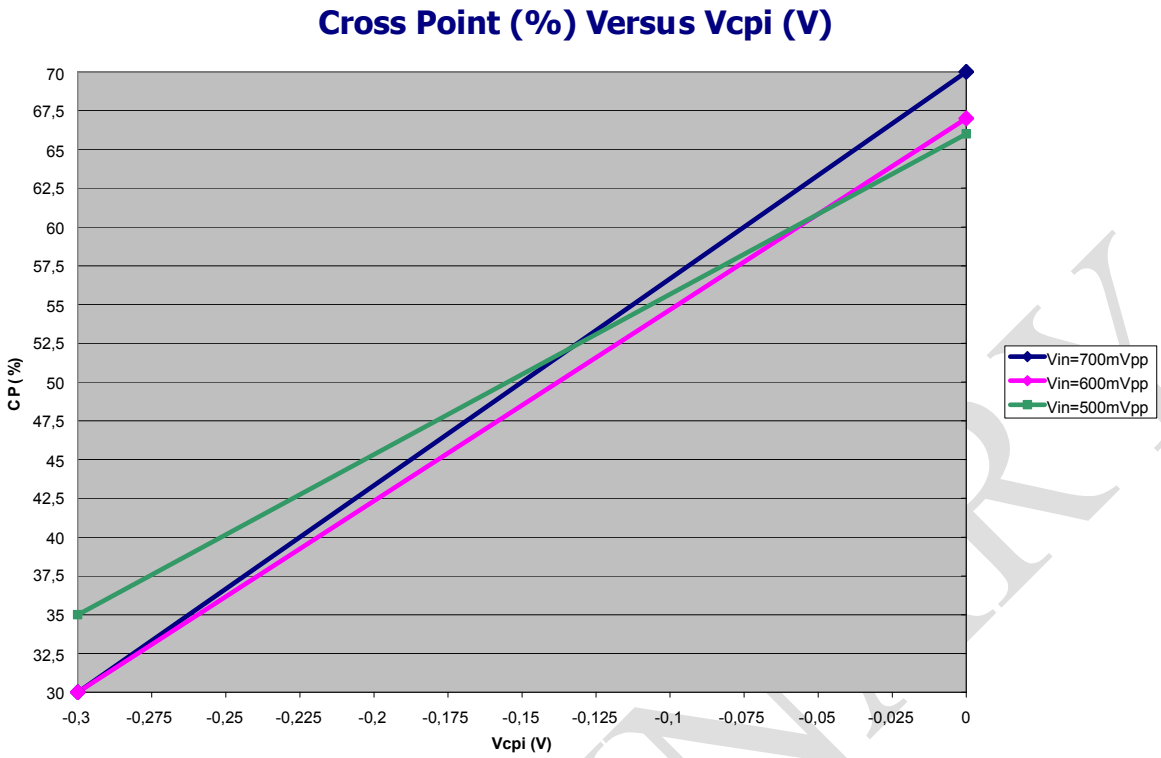
Output Eye Amplitude (V) Versus Vcli (V)



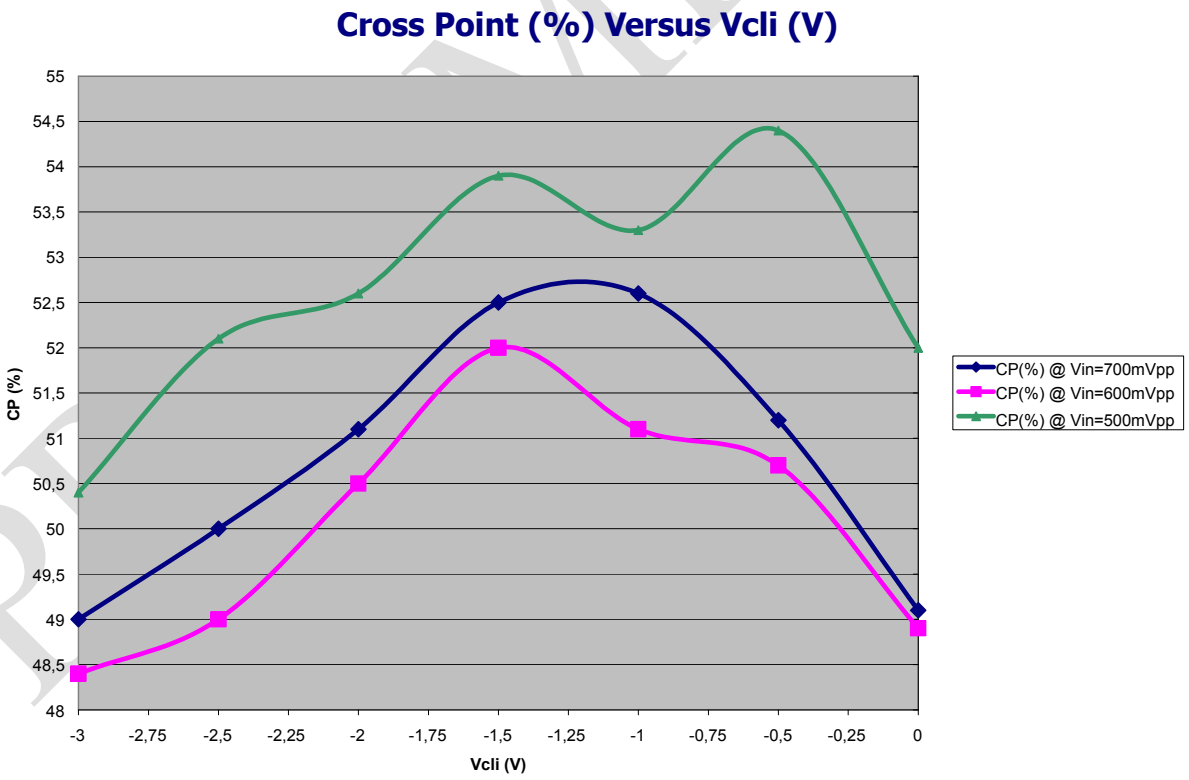
Output voltage eye amplitude variation with output voltage control (for different input levels)

Vdet_i Versus Output amplitude (Vpp)



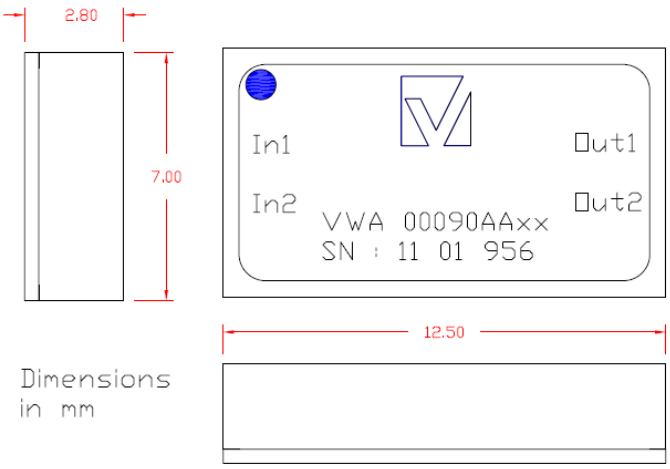


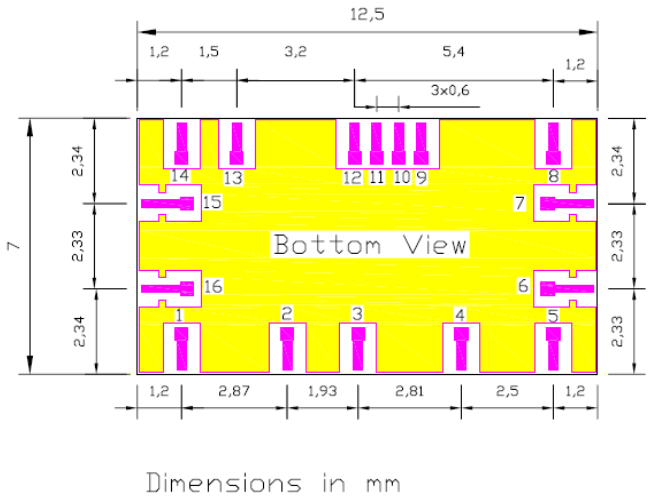
Cross point variation with cross point control (@ Vout=7Vpp)



Cross point variation with output voltage control (when cross point is set at 50% @ Vout=7Vpp)

Mechanical dimensions and pin out





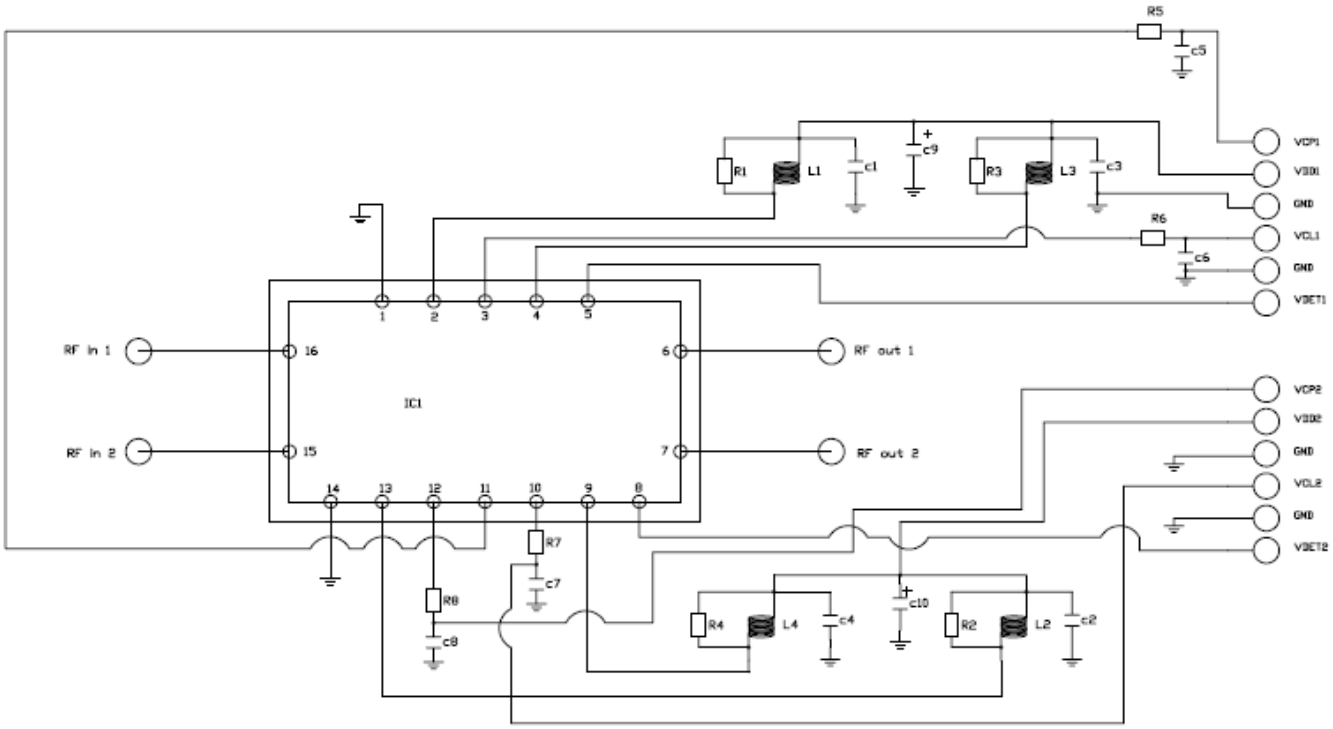
VWA 00090 AAxx P□			
1	GND	9	Vdd22
2	Vdd11	10	Vcl2
3	Vcl1	11	Vcp1
4	Vdd12	12	Vcp2
5	Vdet1	13	Vdd21
6	□ut1	14	GND
7	□ut2	15	In2
8	Vdet2	16	In1

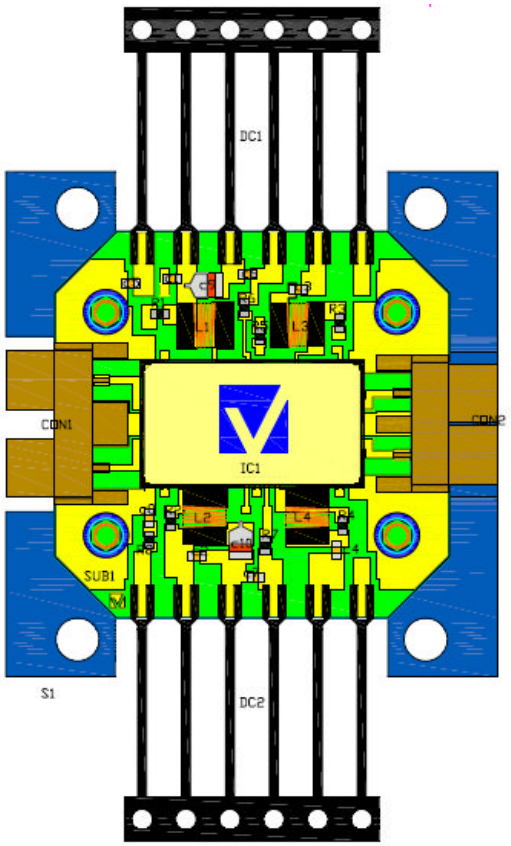
Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the device.

Demonstration board

Demonstration board equipped with low frequencies coils and GPPO connectors is available; ordering code:
VWA 00067 AAxx
Electrical schematic and layout are given bellow.





NEW

10NS-800-DR

High Speed High Current Driver

Description

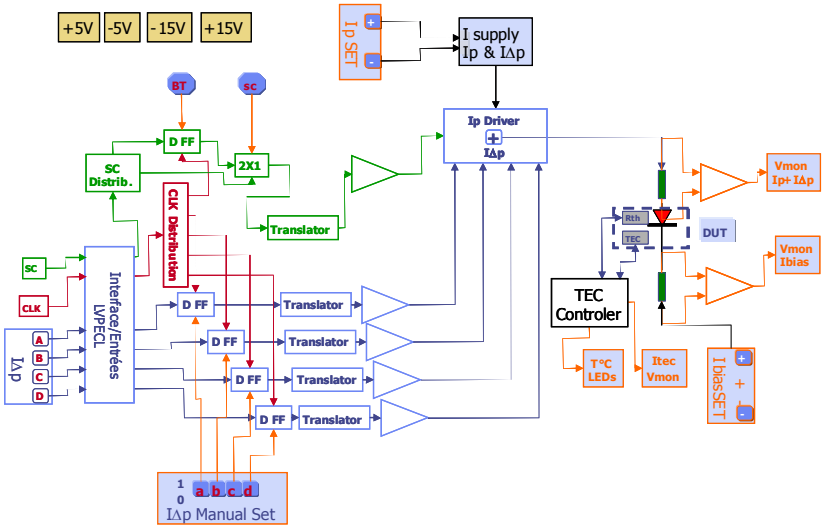
The **10NS-800DR** is a high speed current driver board capable of delivering 800mA in 10ns to an optoelectronic laser or amplifier. The board accepts Butterfly packaged devices with TEC operating parameters up to 2.3V and 3A. The anode and cathode of the optoelectronic device have to be floating (not connected to case). The input control signals are in LVPECL logic, accessible via SMA or 14 pins connector. The current is send to the device when the "Signal Control" is set at logical level one, and trigged on the positive transition of the "Clock" signal. Drive current can be dynamically adjusted thanks to a 4 bits digital control command. Power supply voltages are +/- 5V and +/-15V. The board is equipped with its own heat sink.

Features

- High speed, tr = 10ns typ.
- 800mA drive capability
- On demand current dynamic setting
- Pre bias
- Peak current adjustment
- Manual or dynamic current control
- Synchronization of current switching and level adjustment
- TEC management
- Current monitoring
- Temperature monitoring
- Equipped with heat sink
- 171 x 200 x50 mm

Applications

- Laser driver
- Optical amplifier driver
- Fiber system
- Optical switching



FUNCTIONNAL BLOCK DIAGRAM

Typical Characteristics (ambient 25°C with heat sink)

Medium current setting optoelectronic device serial resistance =3.2 Ohm

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Comment
Positive supply voltage 1	+VDD			+5		V	
Positive supply voltage 2	+VCC			+15		V	
Negative supply voltage 1	-VDD			-5		V	
Negative supply voltage 2	-VCC			-15		V	
Input signal level Low	VxL		1490		1675	mV	Note 1
Input signal level High	VxH		2075		2420	mV	Note 1
Bias current	Ibias	DC pre biasing	0		50	mA	Note 2
Minimum peak Low current	IpL	ABCD=0000 SW7 @ Low	90		220	mA	Note 3
Minimum peak High current	IpH	ABCD=0000 SW7 @ High	90		350	mA	Note 3
Max peak Low current	IpL+ΔIpL	ABCD=1111 SW7 @ Low	140		350	mA	Note 3
Max peak High current	IpH+ΔIpH	ABCD=1111 SW7 @ High	140		560	mA	Note 3
Rise time	Tr	From Ibias to Ip		15	20	ns	Note 4
Fall time	Tf	From Ip to Ibias		15	20	ns	Note 4

Note 1 : LVPECL logic level
Note 2 : manual adjustment with button Ibias Set +/-
Note 3 : ABCD set the added current +ΔIp above Ip. The switch SW7 on board defines 2 working conditions: low current or high current. Current dynamics may be adapted on demand to reach IpH+ΔIpH = 800mA.
Note 4 : measured on resistive load

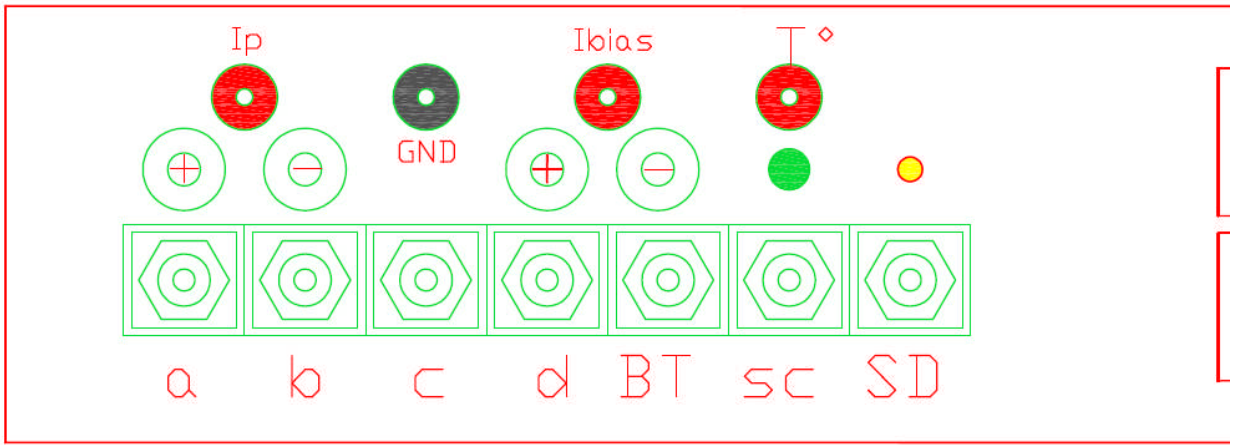
Environment Parameters		Symbols	Min	Max	Units
Operating temperature	Under air flow	T_{op}	0	+45	°C
Storage temperature		T_{stg}	- 40	+85	°C

Absolute maximum ratings

Maximum ratings	Symbols	Min	Max	Units
Positive supply voltage 1	+VDD	4.75	5.25	V
Positive supply voltage 2	+VCC	14.25	15.75	V
Negative supply voltage 1	-VDD	-5.25	-4.75	V
Negative supply voltage 2	-VCC	-15.75	-14.25	V
Input signals		0	3.1	V

Front panel controls

Name	Symbol	Function
Test Button	BT	Active when in "1" position : allow a,b,c and d manual setting, Ip manual setting, Ip monitoring and CW current drive (Ip+Δip)
Trig enable	sc	Disable Clk trigger function when in logical "1".
Manual A set	a	Defines A (Δip) value for testing, when BT = "1".
Manual B set	b	Defines B (Δip) value for testing, when BT = "1".
Manual C set	c	Defines C (Δip) value for testing, when BT = "1".
Manual D set	d	Defines D (Δip) value for testing, when BT = "1".
Current monitoring	Ip	Access to a voltage value image of the current (total)
Ip setting +	Ip +	Pushing the Ip+ button will increase the Ip value (64 steps)
Ip setting -	Ip -	Pushing the Ip- button will decrease the Ip value (64 steps)
Groung	GND	Ground reference for Ip and T°C voltage
Bias current monitoring	Ibias	Access to a voltage value image of the bias current Ibias
Ibias setting +	Ibias +	Pushing the Ibias+ button will increase the Ibias value (64 steps)
Ibias setting -	Ibias -	Pushing the Ibias- button will decrease the Ibias value (64 steps)
Temperature monitoring	T°	Access to a voltage value image of the optoelectronic device. LED color code : green = 25°C, blue <24°C, red>26°C
Stand by	SD	Stand by mode, no control, no current, low power consumption.

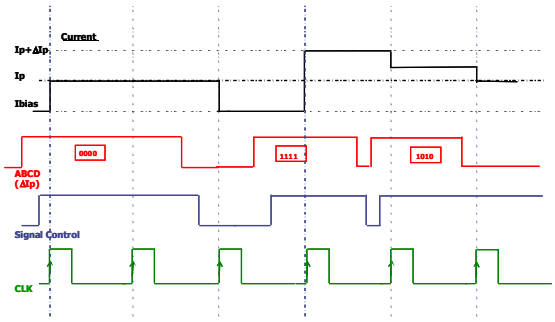


Signals description

Signal	Symbol	Function
Signal Control	SC	Automatic mode (sc switch at 0):"1" level allows current Ip to pass in optoelectronic device, trigged on positive transition of Clock signal. Logical "0" level stops the current. Semi-automatic mode (sc switch at 1): No trigger function of Clock signal. A "1" level allows current Ip to pass in optoelectronic device. Logical "0" level stops the current.
Clock	Clk	Active on positive transition. On automatic mode, synchronizes SCl, A, B, C and D signals.
Amplitude control A	A	Bit 1 - LSB (among 4) defining current increase ΔIp above Ip.
Amplitude control B	B	Bit 2 (among 4) defining current increase ΔIp above Ip.
Amplitude control C	C	Bit 3 (among 4) defining current increase ΔIp above Ip.
Amplitude control D	D	Bit 4 - MSB (among 4) defining current increase ΔIp above Ip.

Truth table and chronogram

Input Signals (LVPECL)						Switchs Front Panel						
SC	A	B	C	D	CLK	BT	sc	a	b	c	d	I (Current)
0	X	X	X	X	X	0	0	0	0	0	0	Ibias
1	0	0	0	0	⤴	0	0	0	0	0	0	Ibias + Ip
1	A	B	C	D	⤴	0	0	0	0	0	0	Ibias + Ip + IΔp
X	X	X	X	X	X	1	X	0	0	0	0	Ibias + Ip
X	X	X	X	X	X	1	X	a	b	c	d	Ibias + Ip + IΔp
0	X	X	X	X	X	0	1	0	0	0	0	Ibias
1	0	0	0	0	X	0	1	0	0	0	0	Ibias + Ip
1	A	B	C	D	X	0	1	0	0	0	0	Ibias + Ip
1	A	B	C	D	⤴	0	1	0	0	0	0	Ibias + Ip + IΔp



Current dynamics

Figures 1 and 2 show the Ip and ΔIp maximum current dynamics for two different board settings.

Ip is set manually between IpL and IpH using Ip+ / Ip- buttons. The Ip value is automatically stored in a non volatile memory. Current value can be monitored through a test point (connect a volt meter).

On board switch "SW7" splits the current dynamic in two parts, with a ratio of 2 for the maximum current.

Figures 1 and 2 bellow show the current Ip+ΔIp (mA) as function of Ip and ΔIp commands.

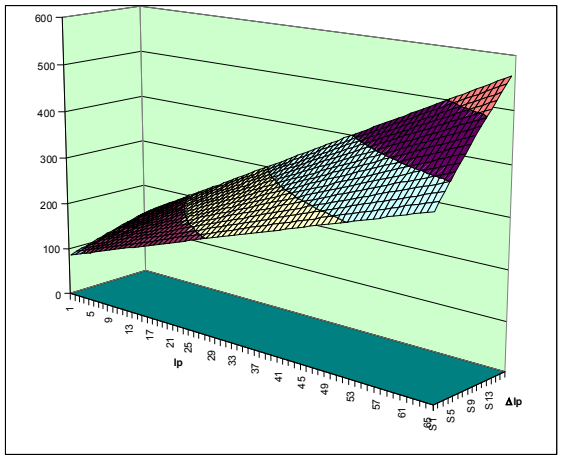


Fig 1 : Medium current setting dynamics

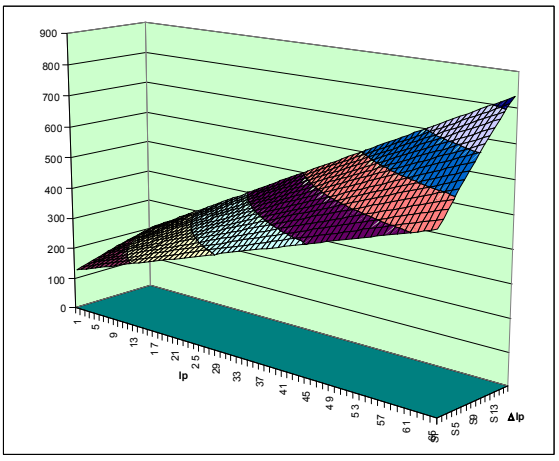
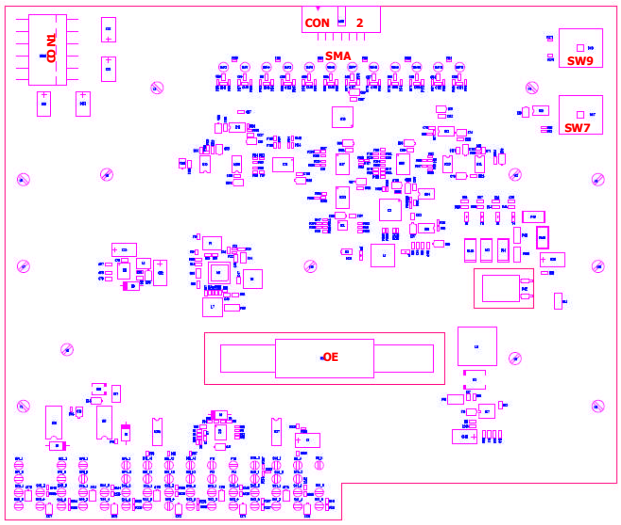


Fig 2 : High current setting dynamics



OE is fixed on heat sink with four 2mm screws.

CON1	Power supply connector (6pins)
CON2	Signal connector (14 pins)
SMA	SMA signal connectors 2x6
SW7	Current dynamic setting Low/High
SW9	TEC current and voltage setting Low/High
OE	Optoelectronic device

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **10NS-800DR** module.
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

Ordering information

Product code	Max peak current
VLI 00005 AA	560 mA
VLI 00005 AD	800 mA

End Document